

FIG. 1A

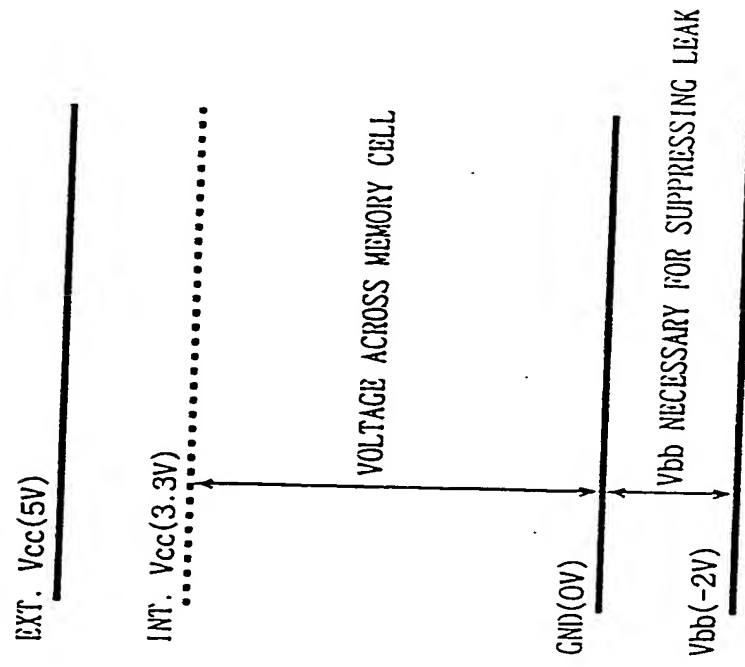


FIG. 1B

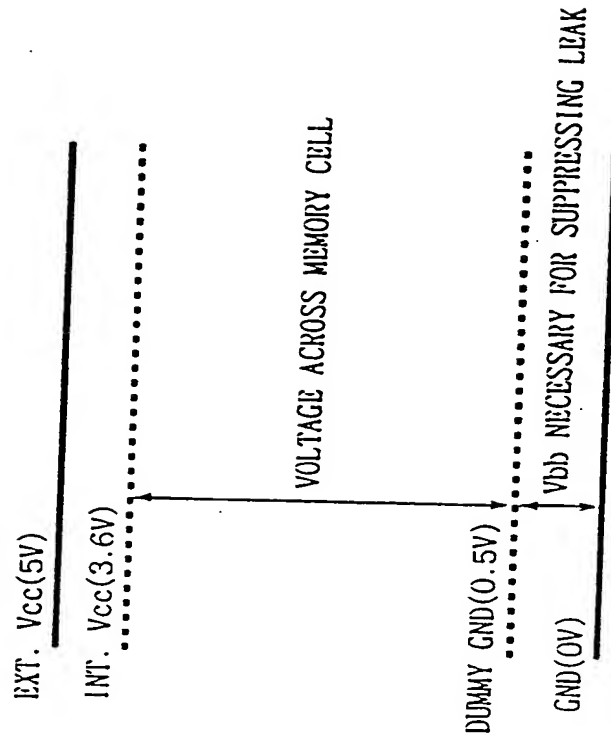


FIG. 2

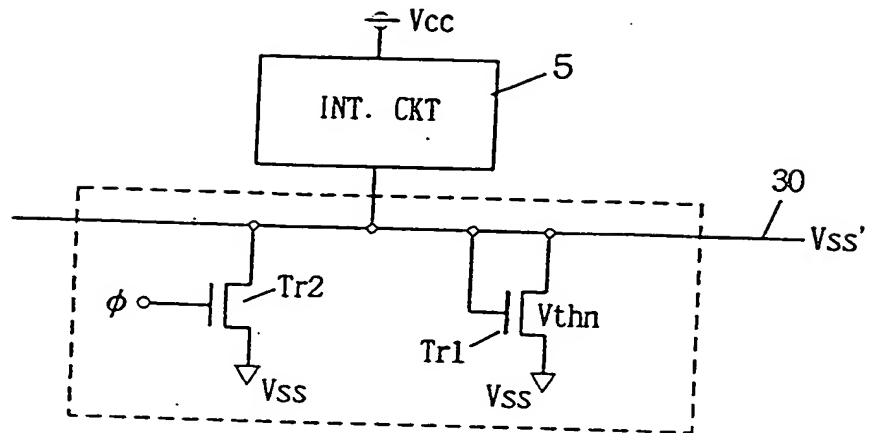


FIG. 3

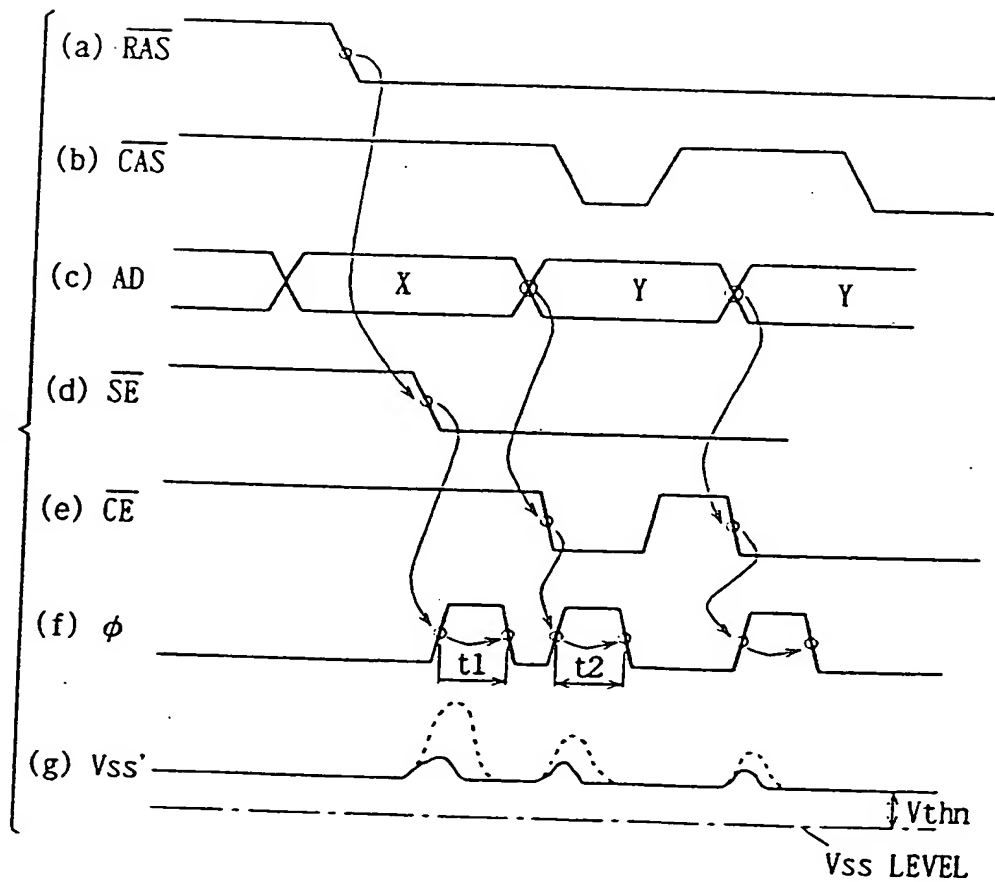


FIG. 4

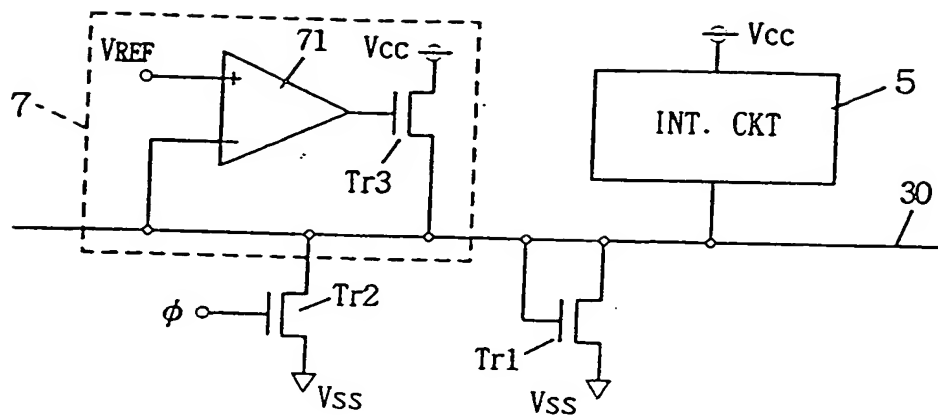


FIG. 5

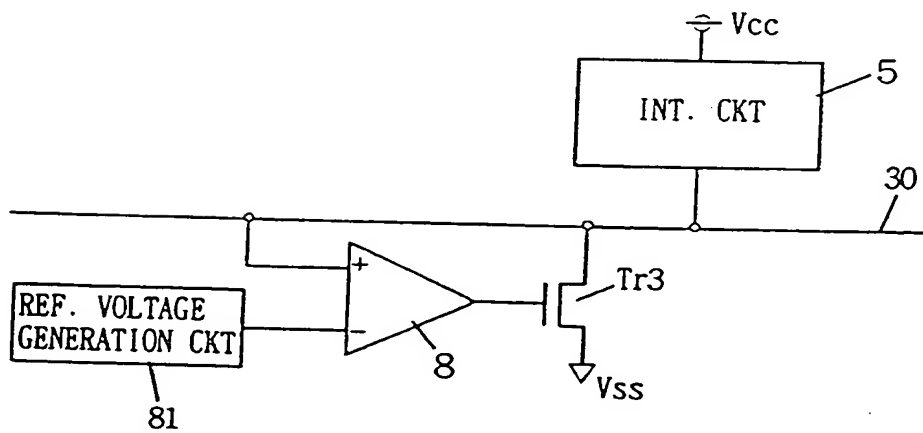


FIG. 6

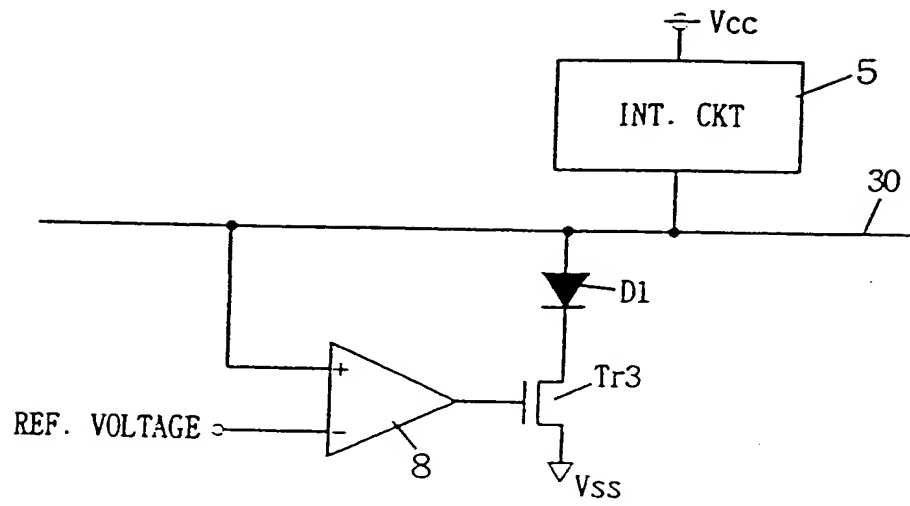


FIG. 7

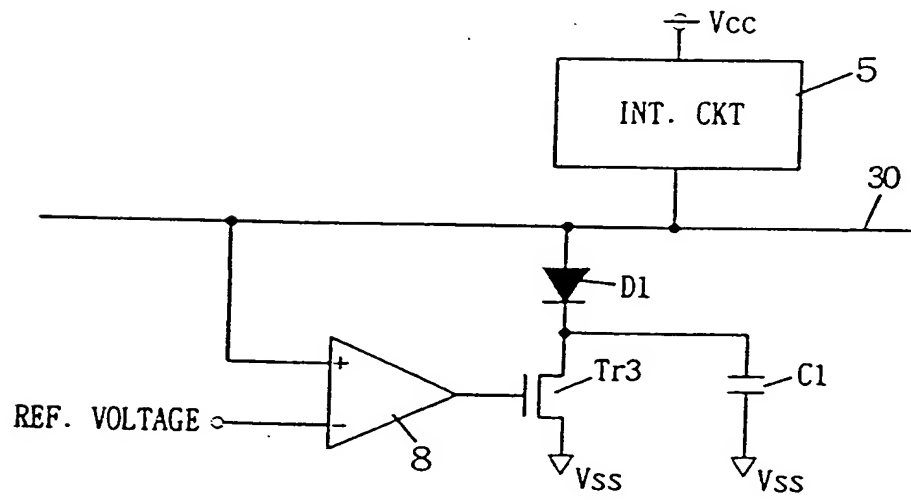


FIG. 8

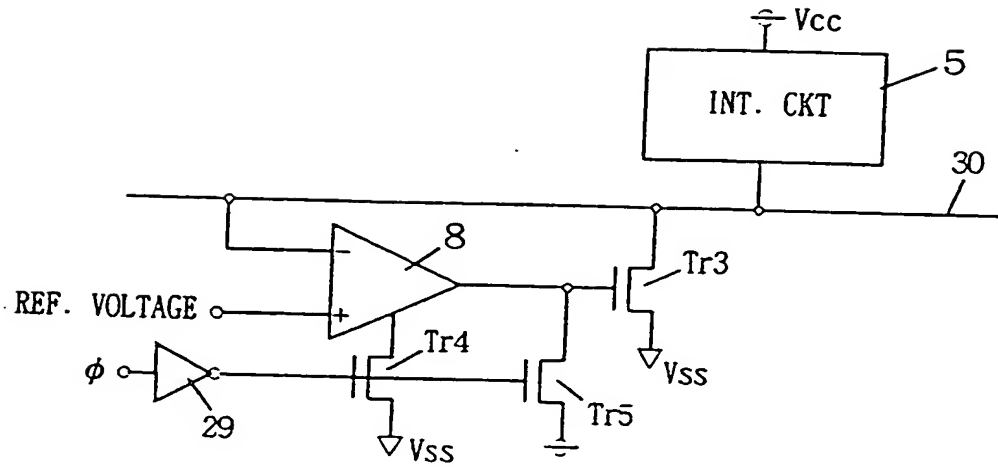


FIG. 9

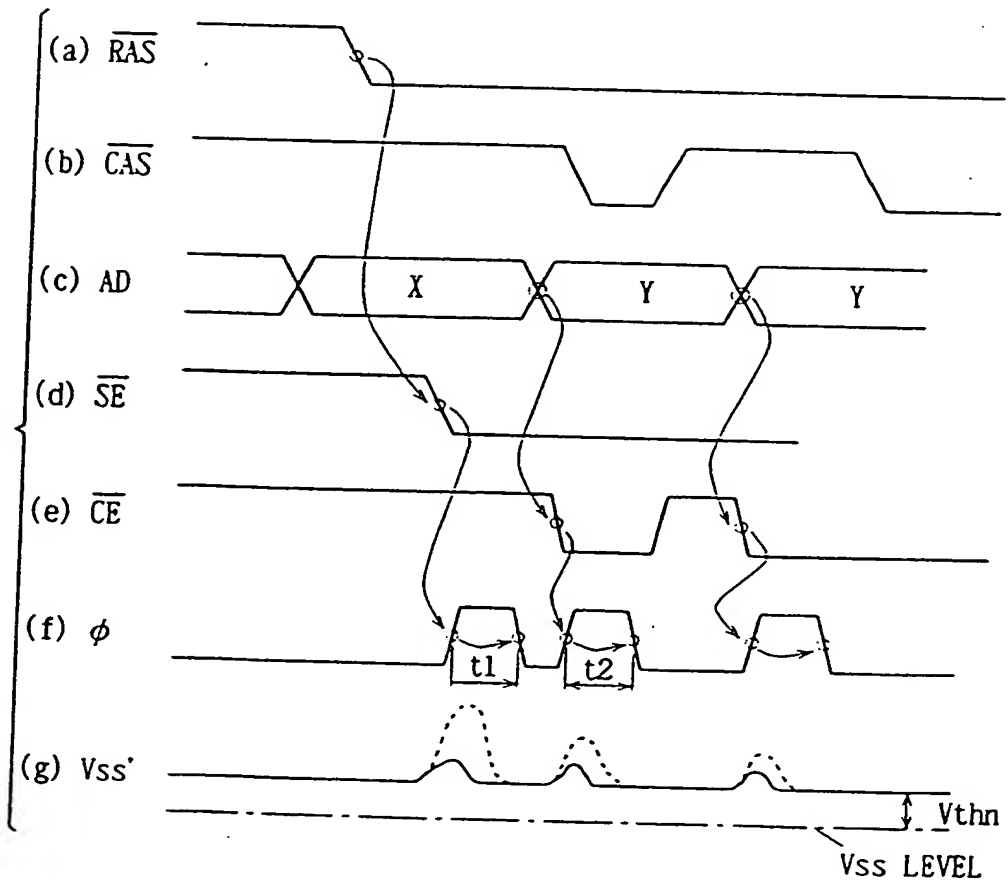


FIG. 10

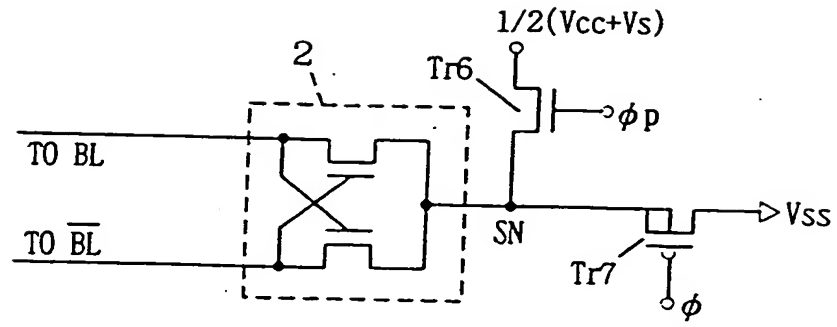


FIG. 11

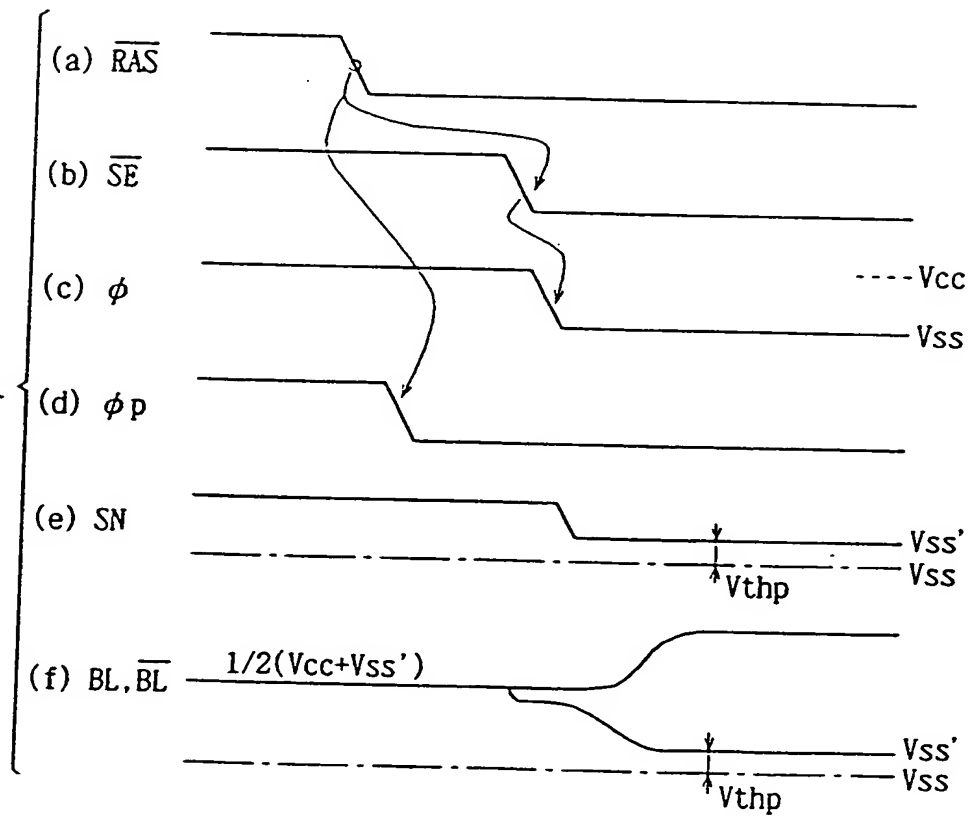


FIG. 12

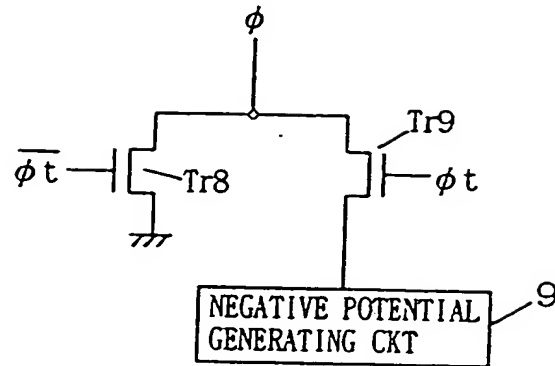
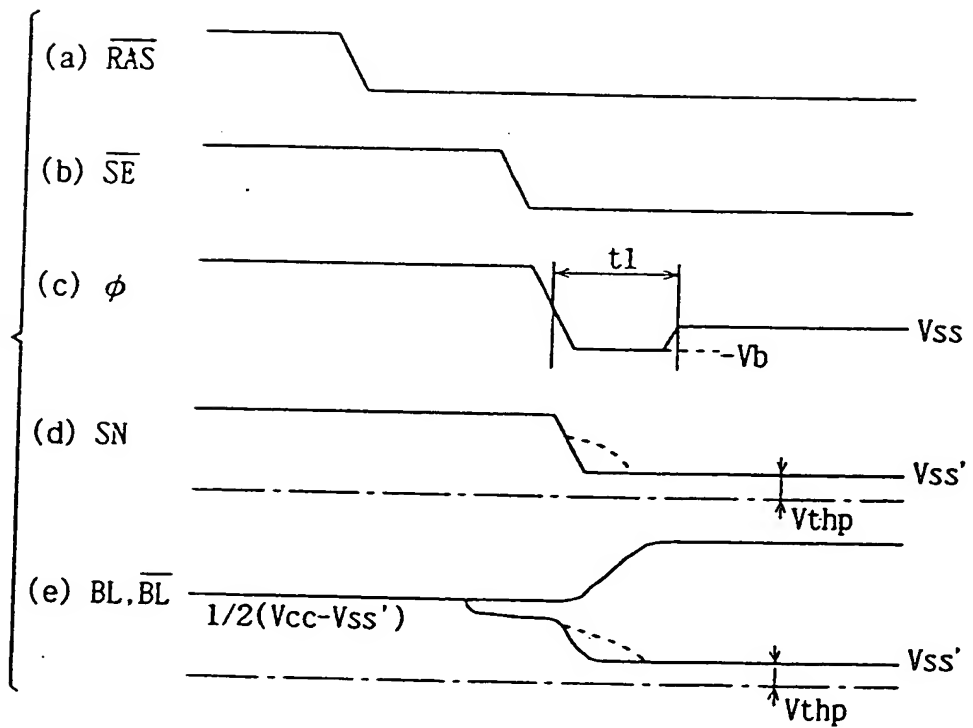


FIG. 13



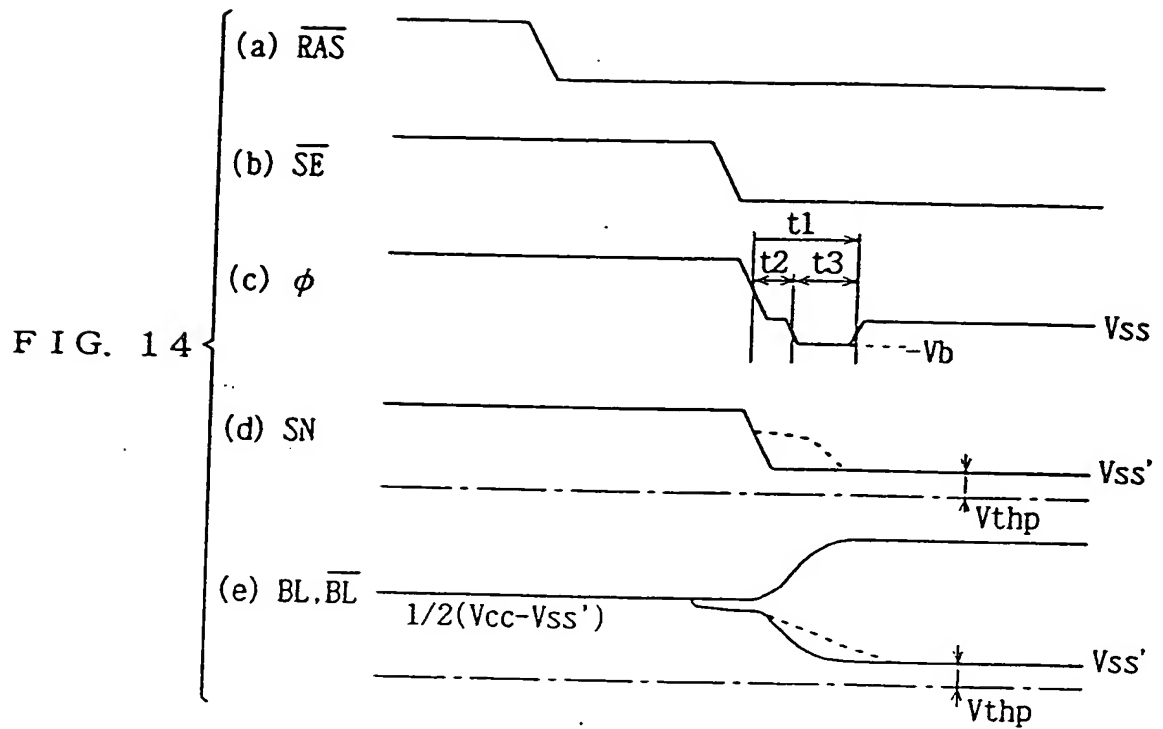


FIG. 15

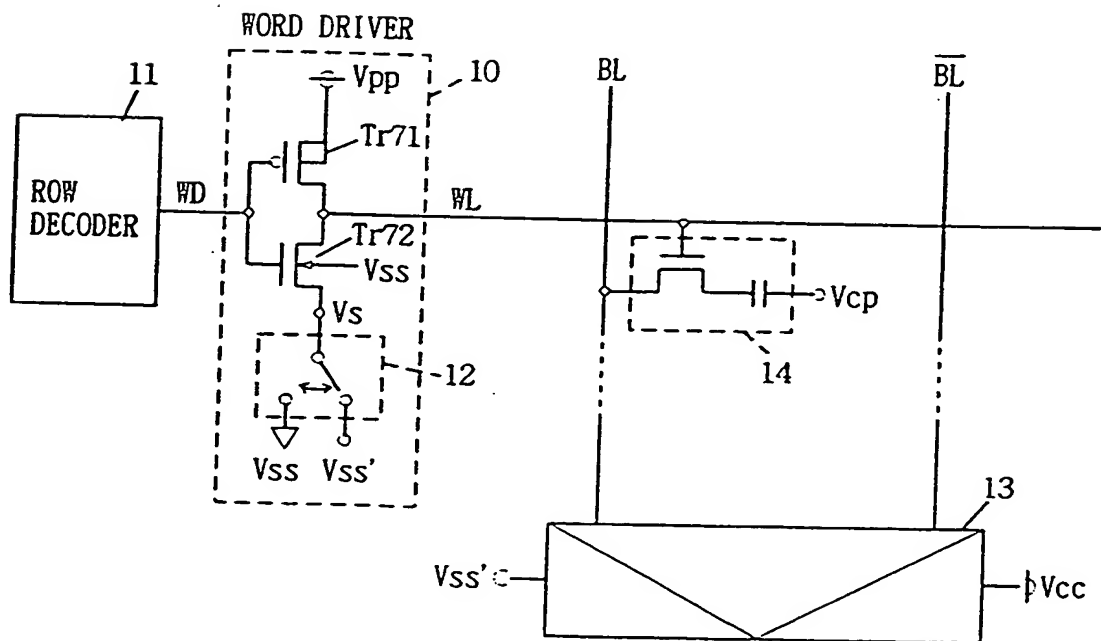


FIG. 16

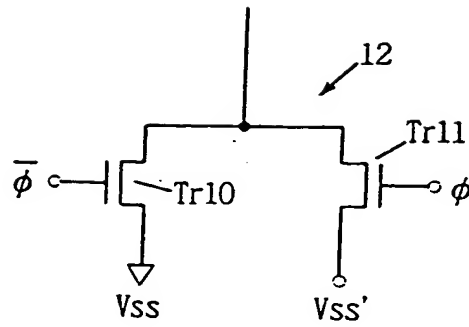
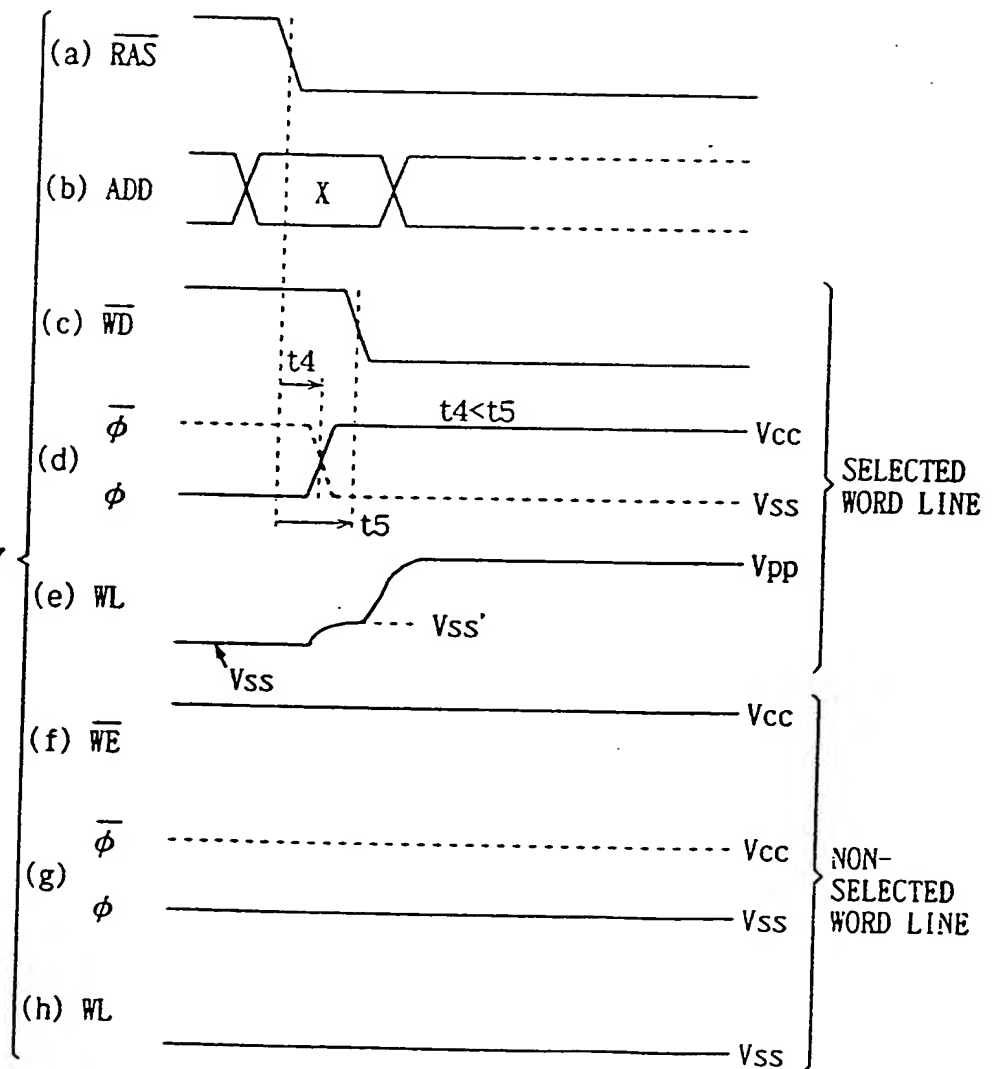


FIG. 17



[illegible]

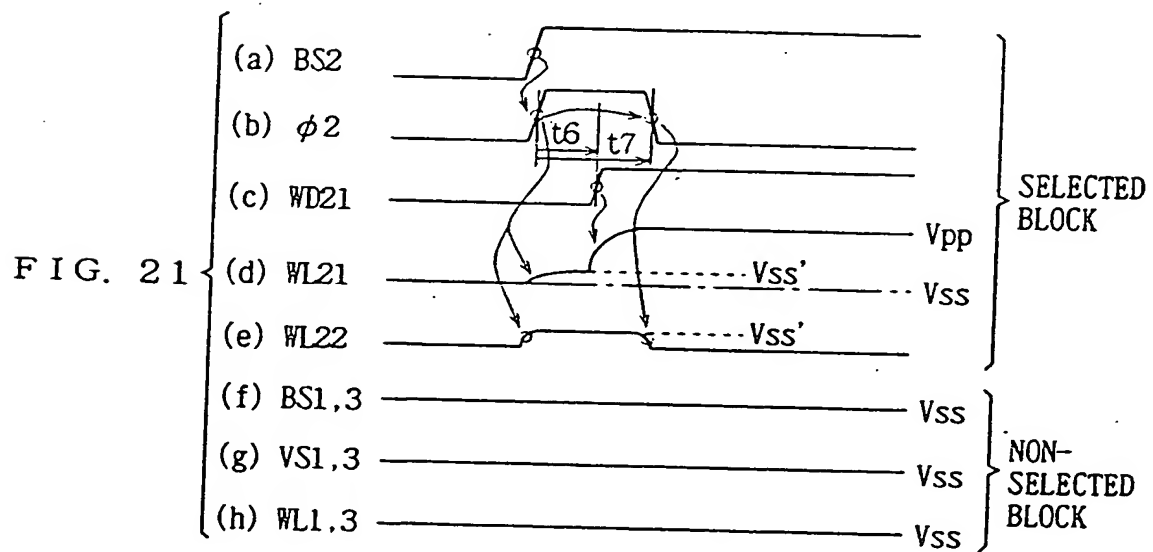
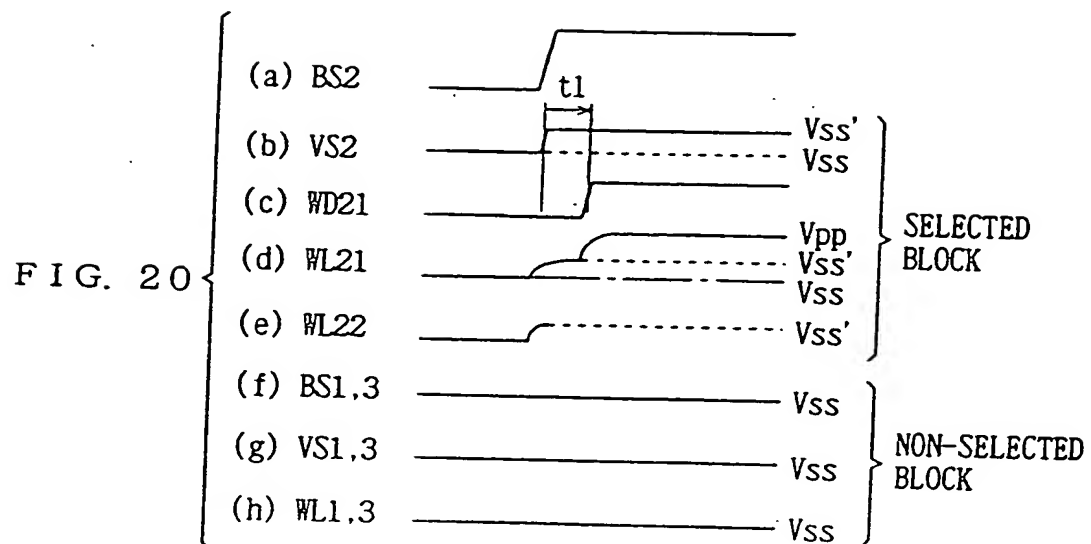


FIG. 22

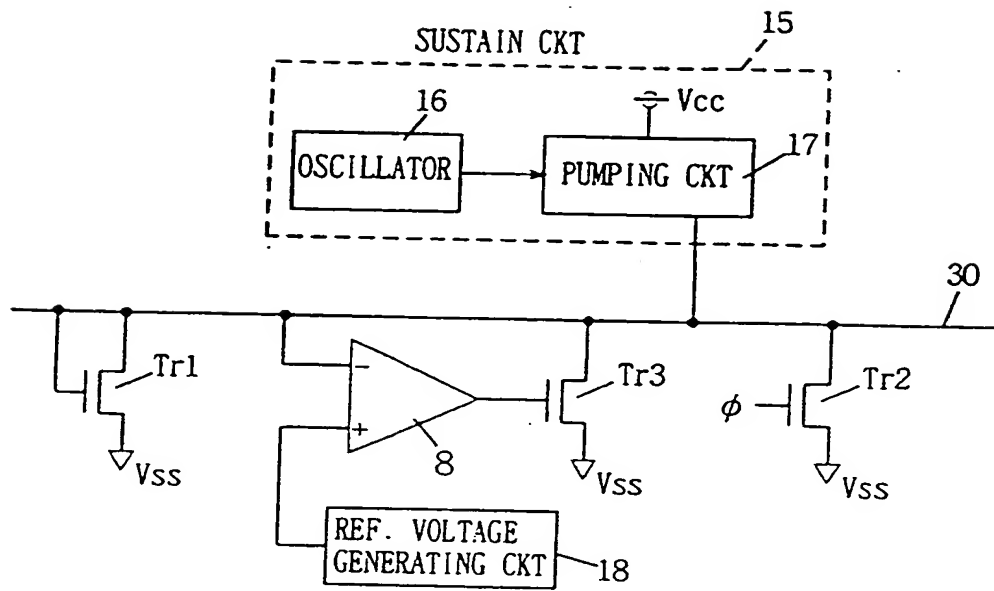
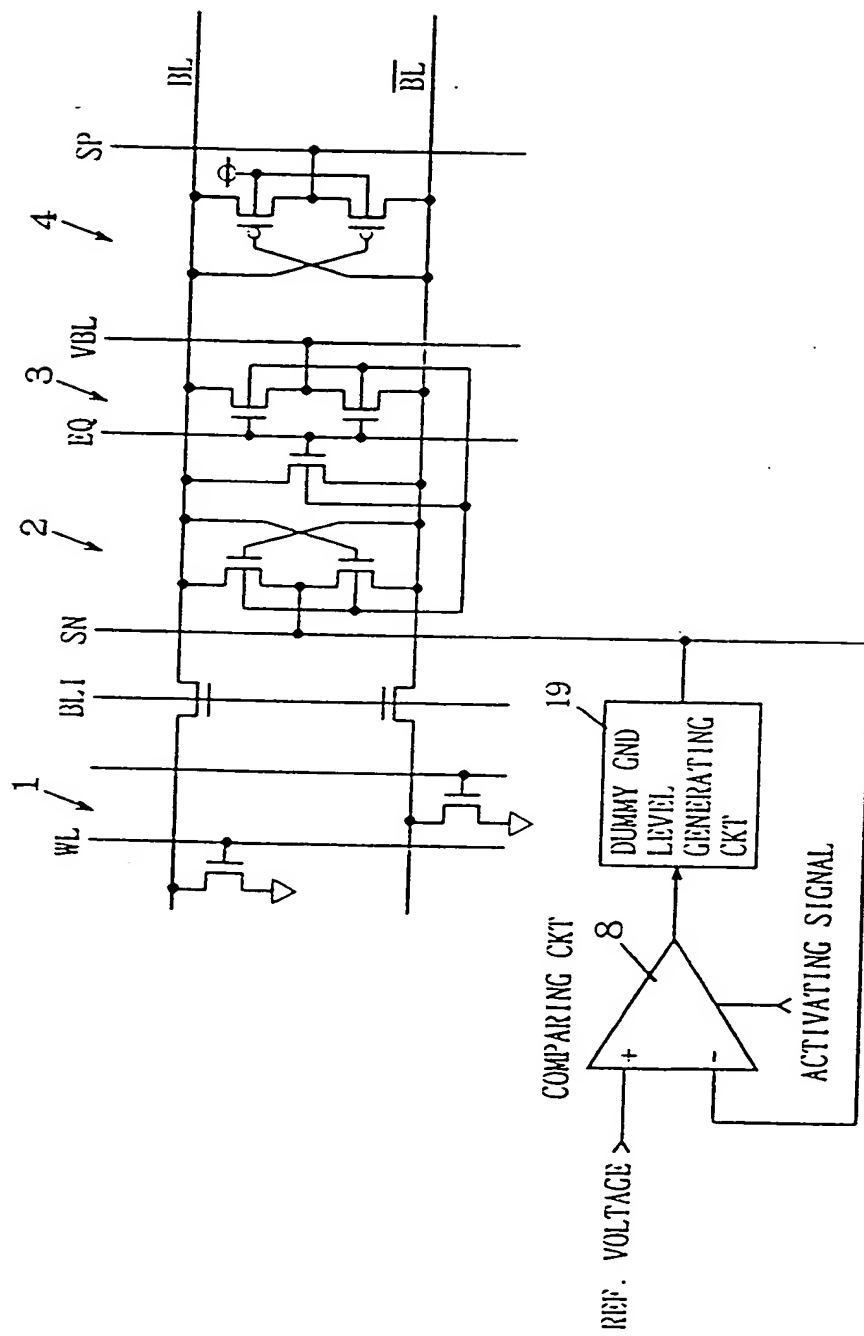


FIG. 23



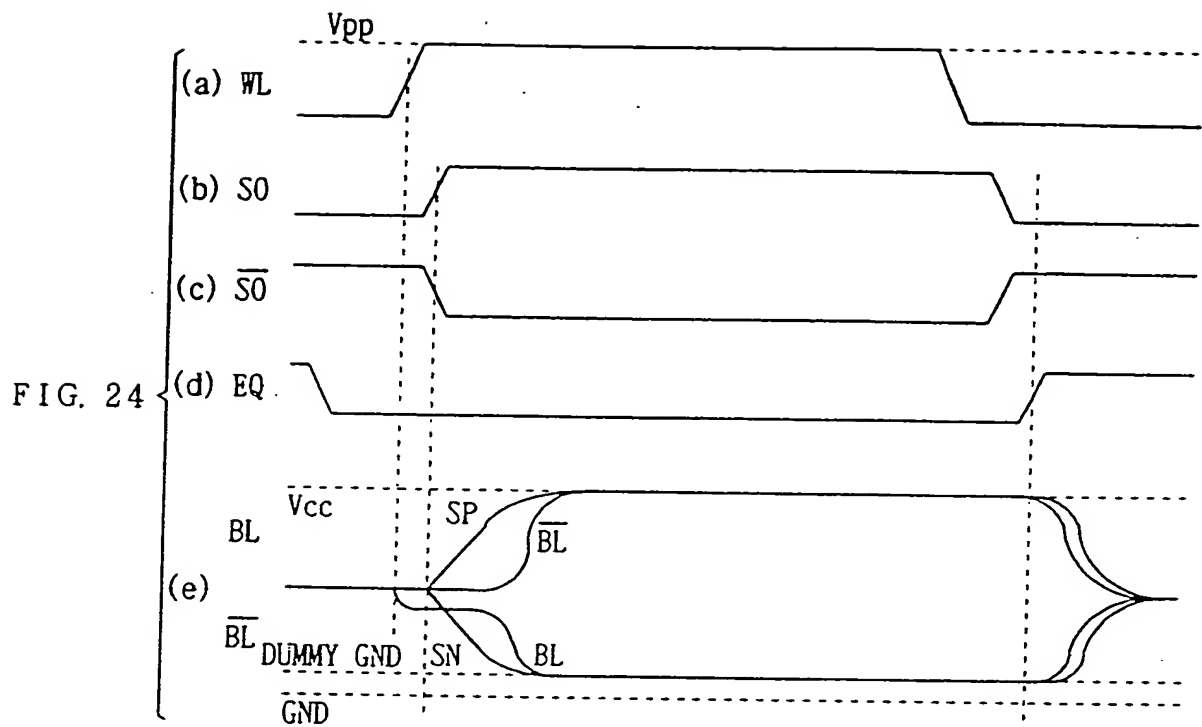


FIG. 25

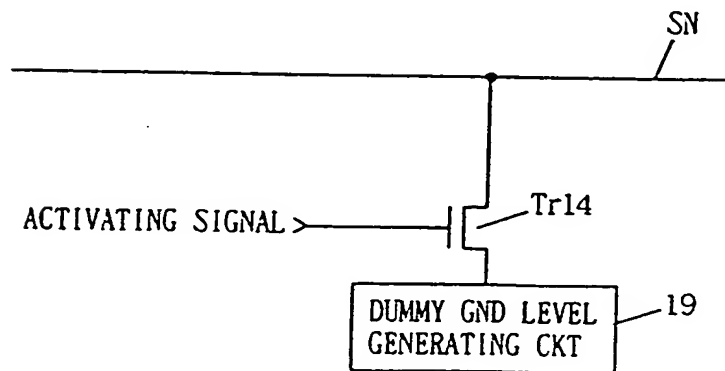


FIG. 26

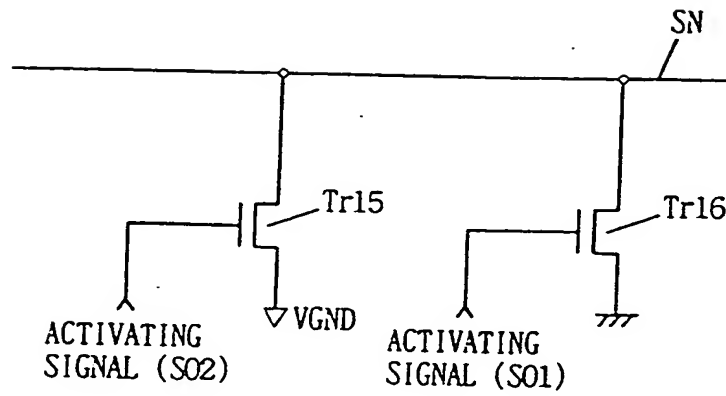


FIG. 27

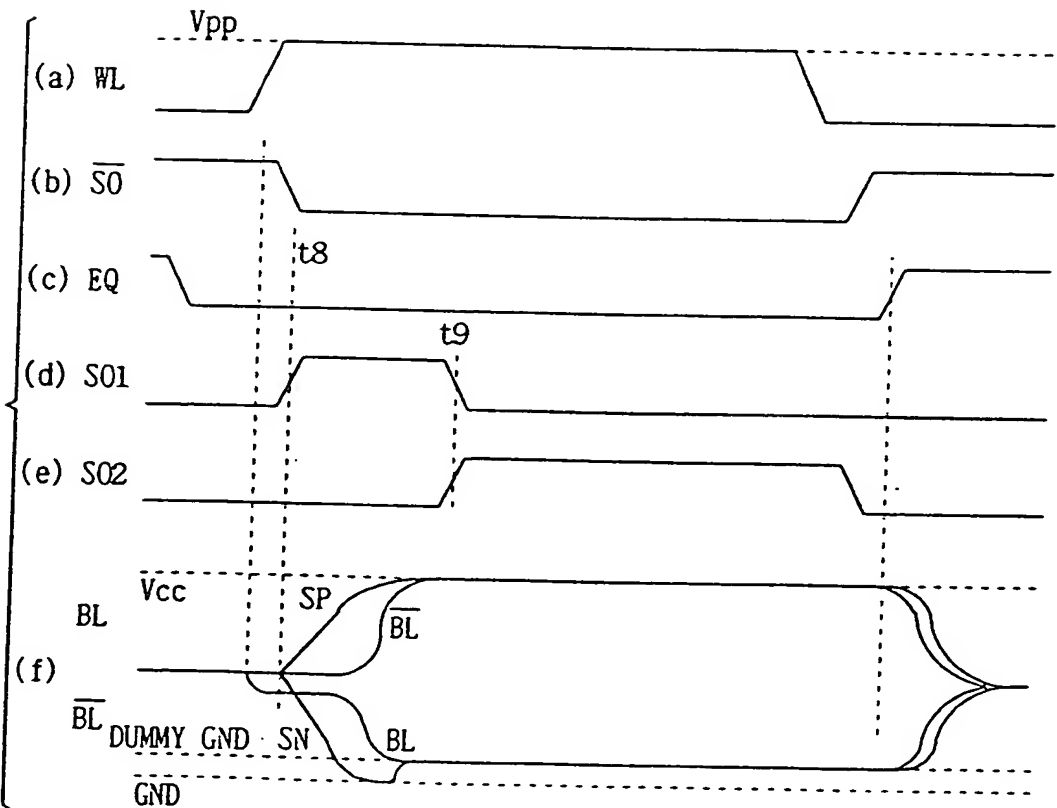


FIG. 28

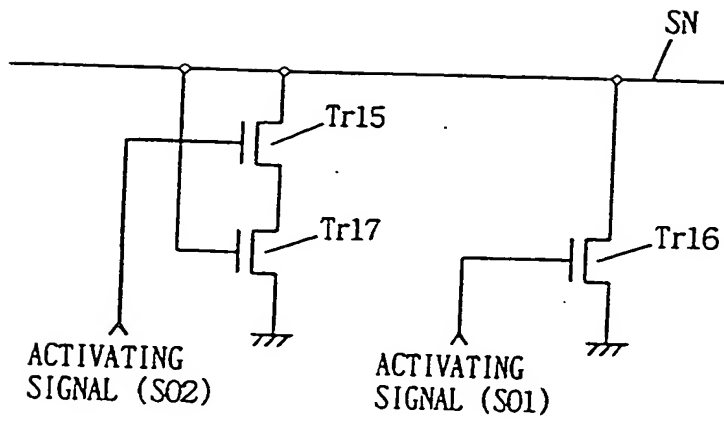


FIG. 29

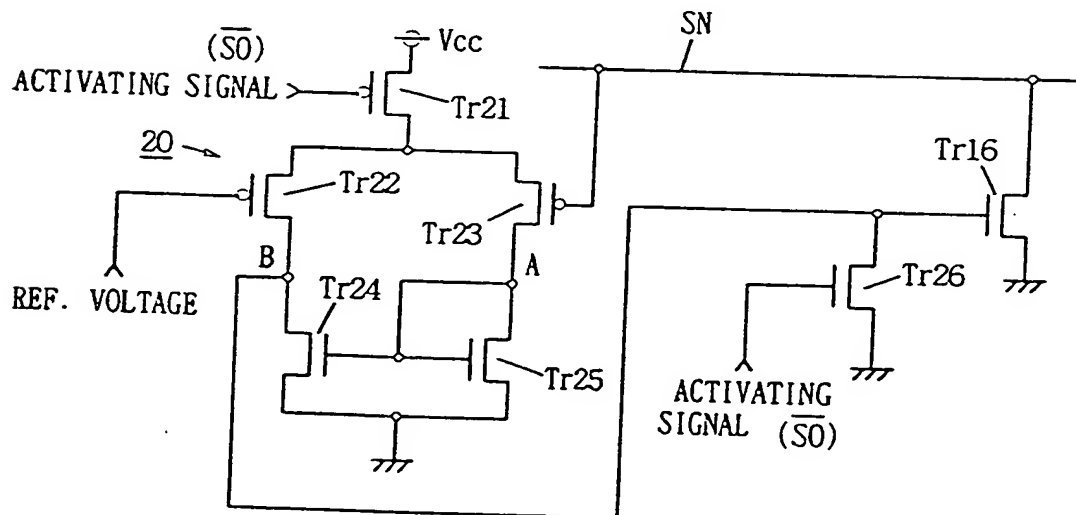


FIG. 30

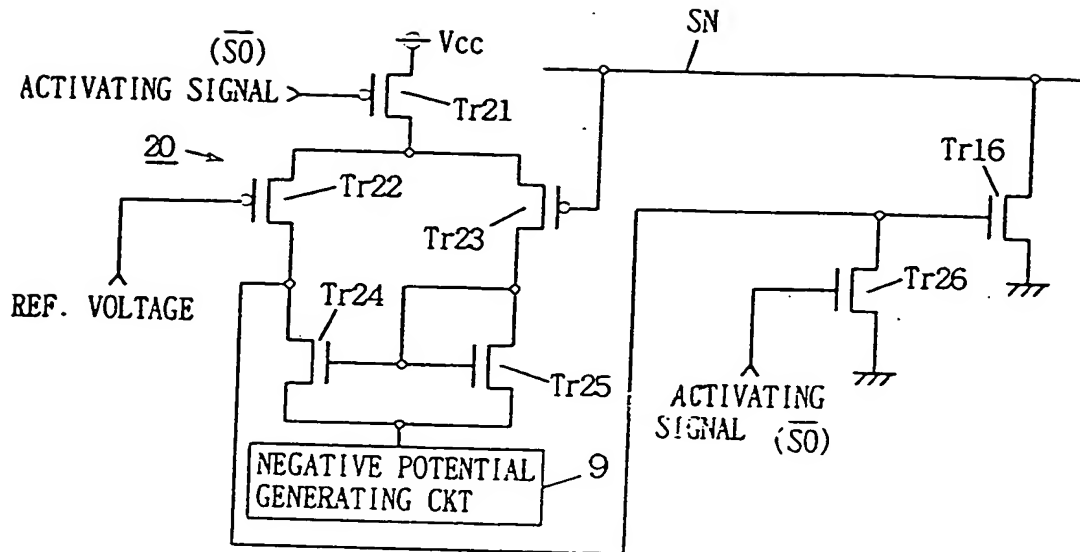


FIG. 31

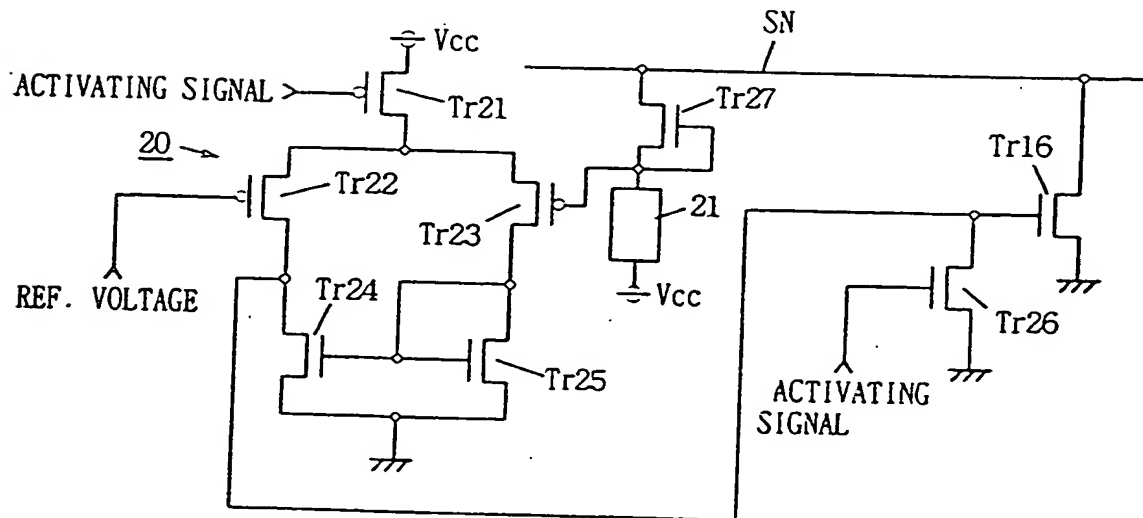


FIG. 32

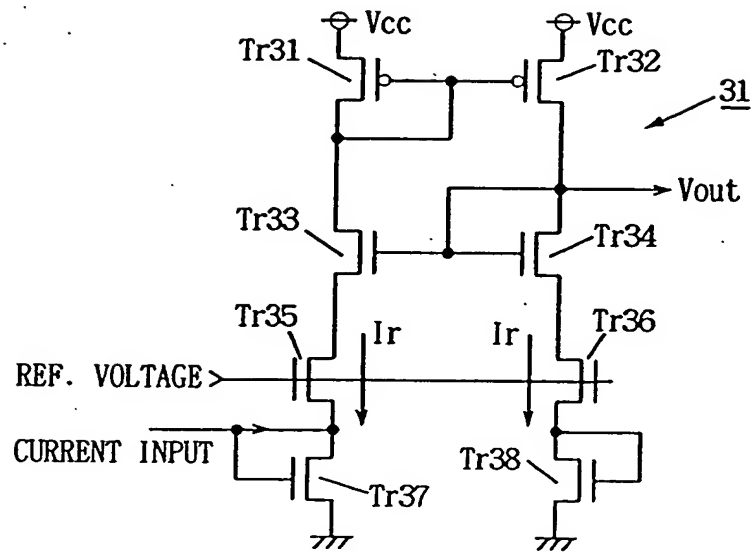


FIG. 33

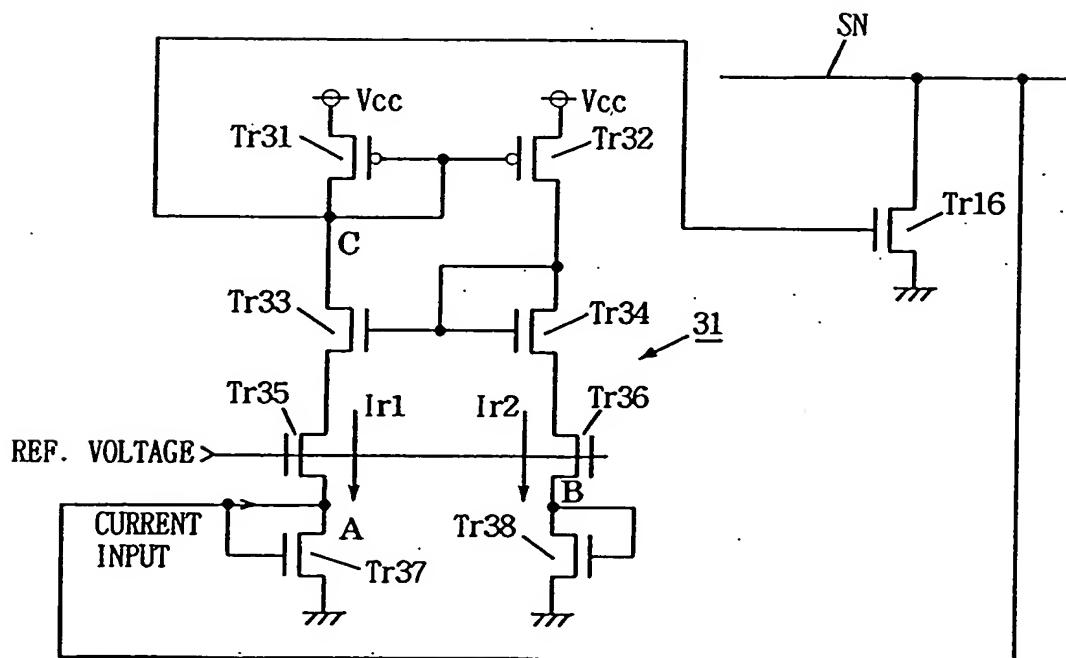


FIG. 34

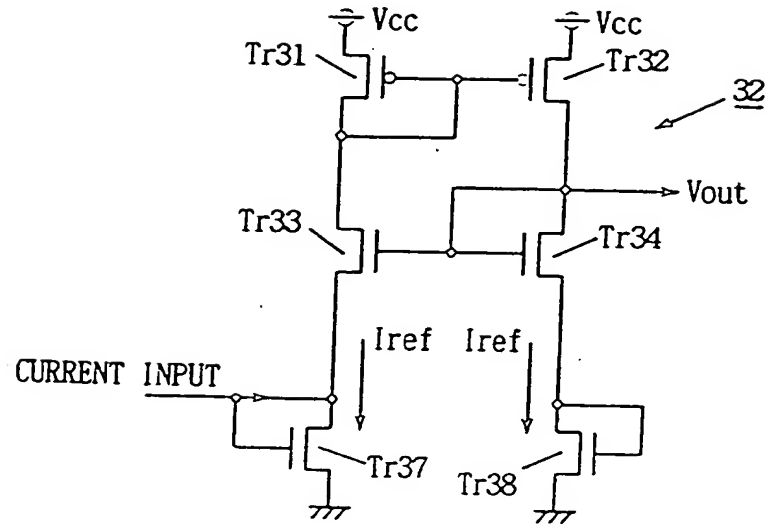


FIG. 35

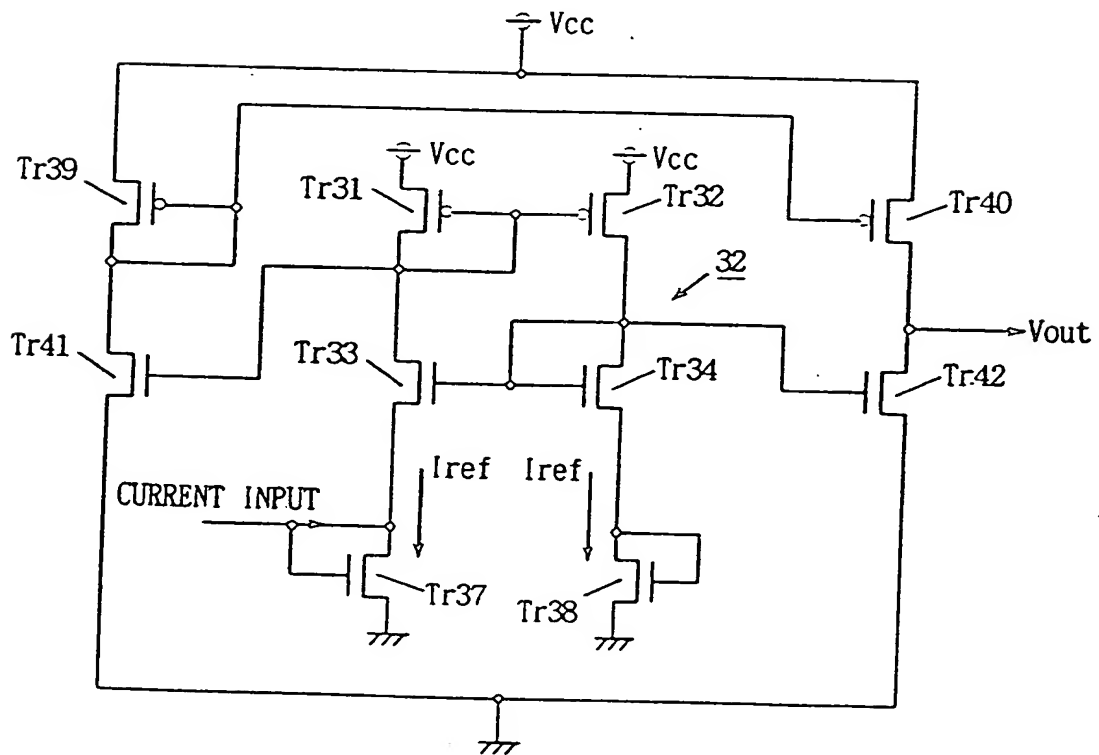


FIG. 36

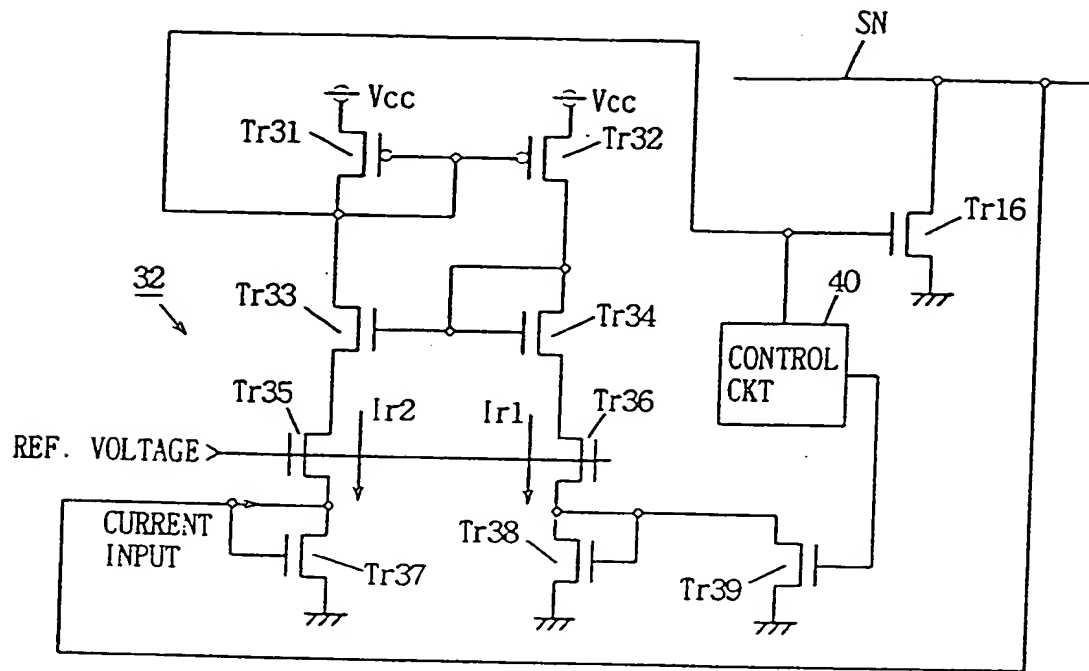


FIG. 37

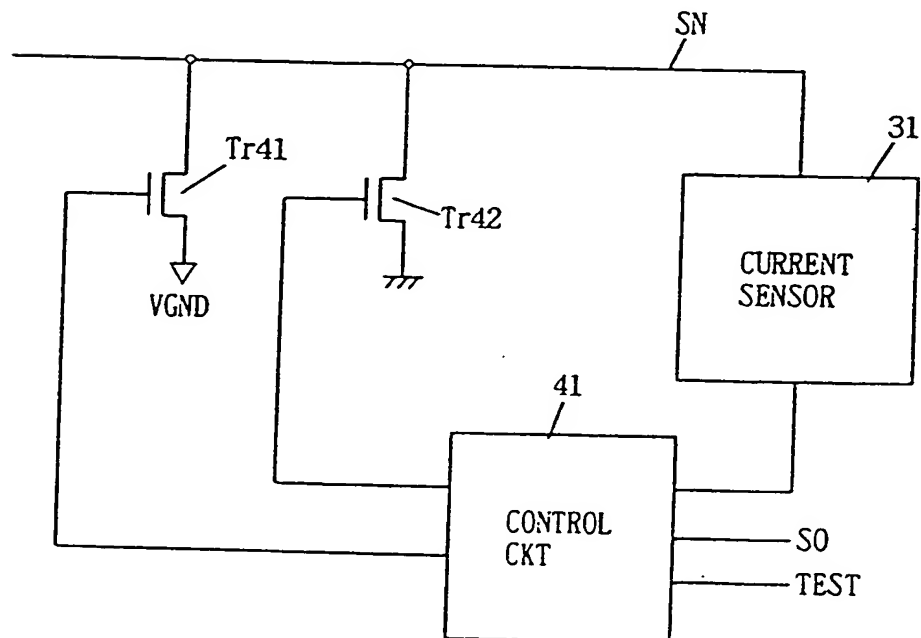


FIG. 38

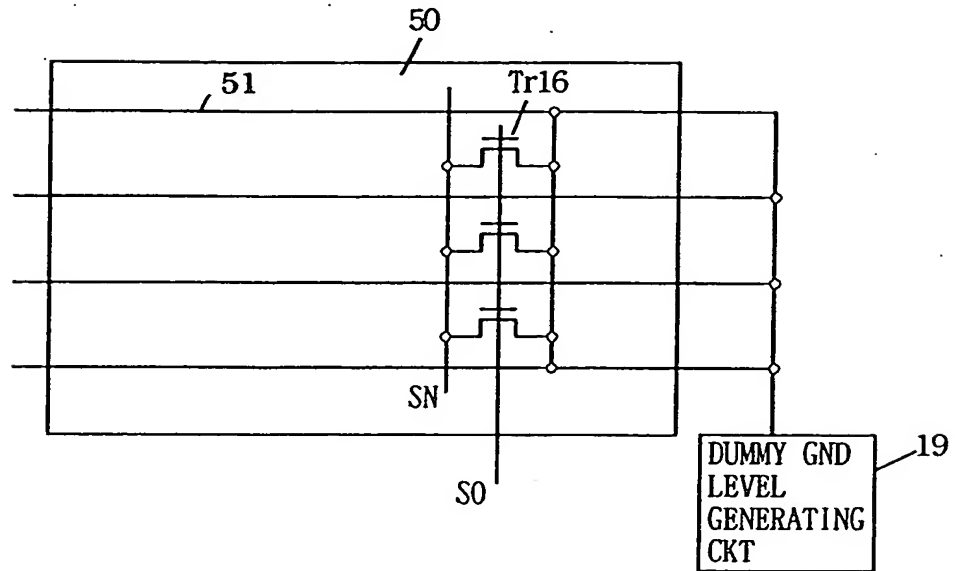


FIG. 39

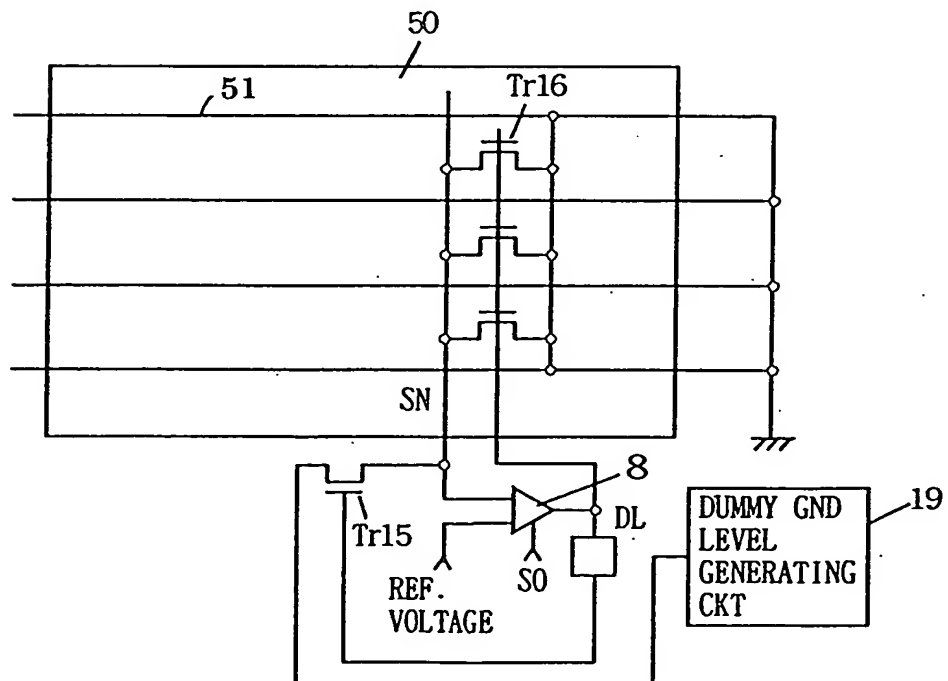


FIG. 40

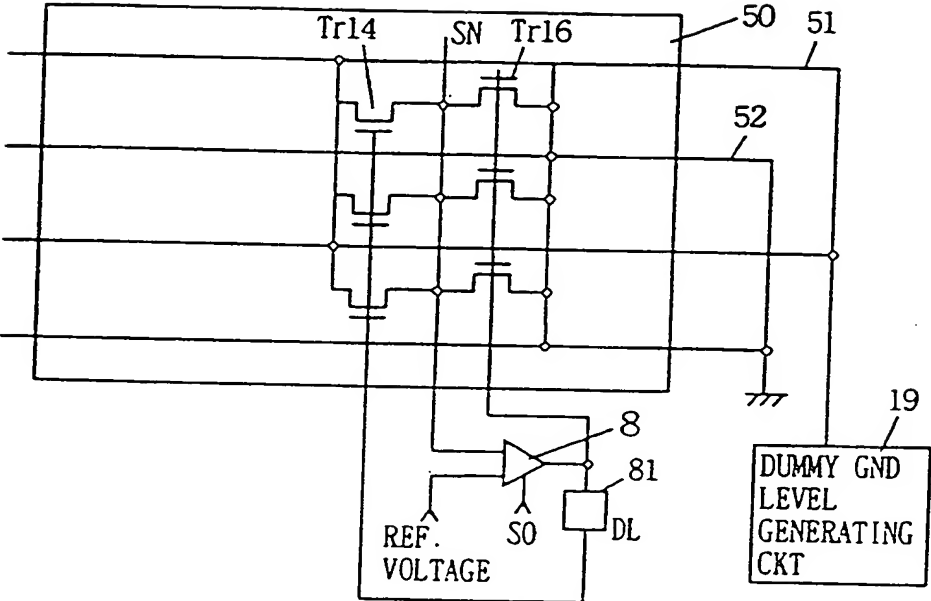
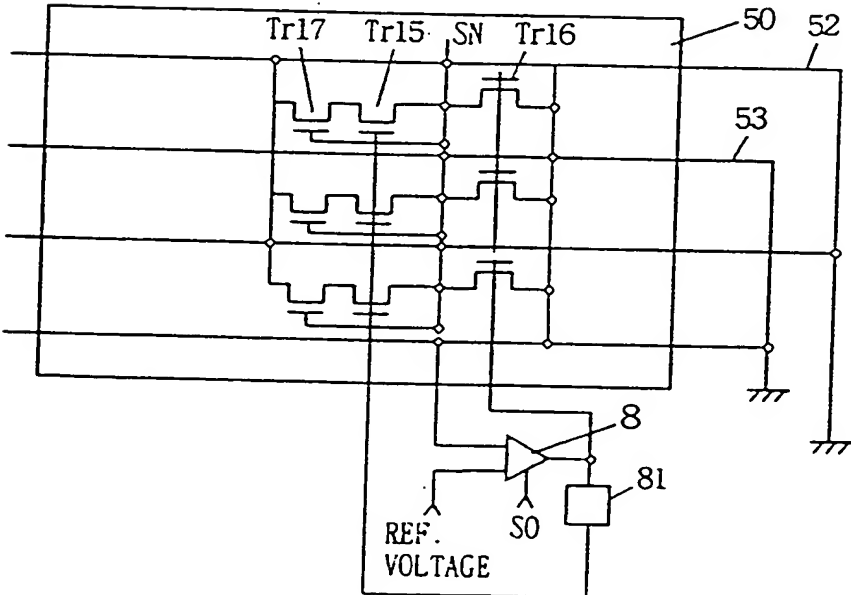


FIG. 41



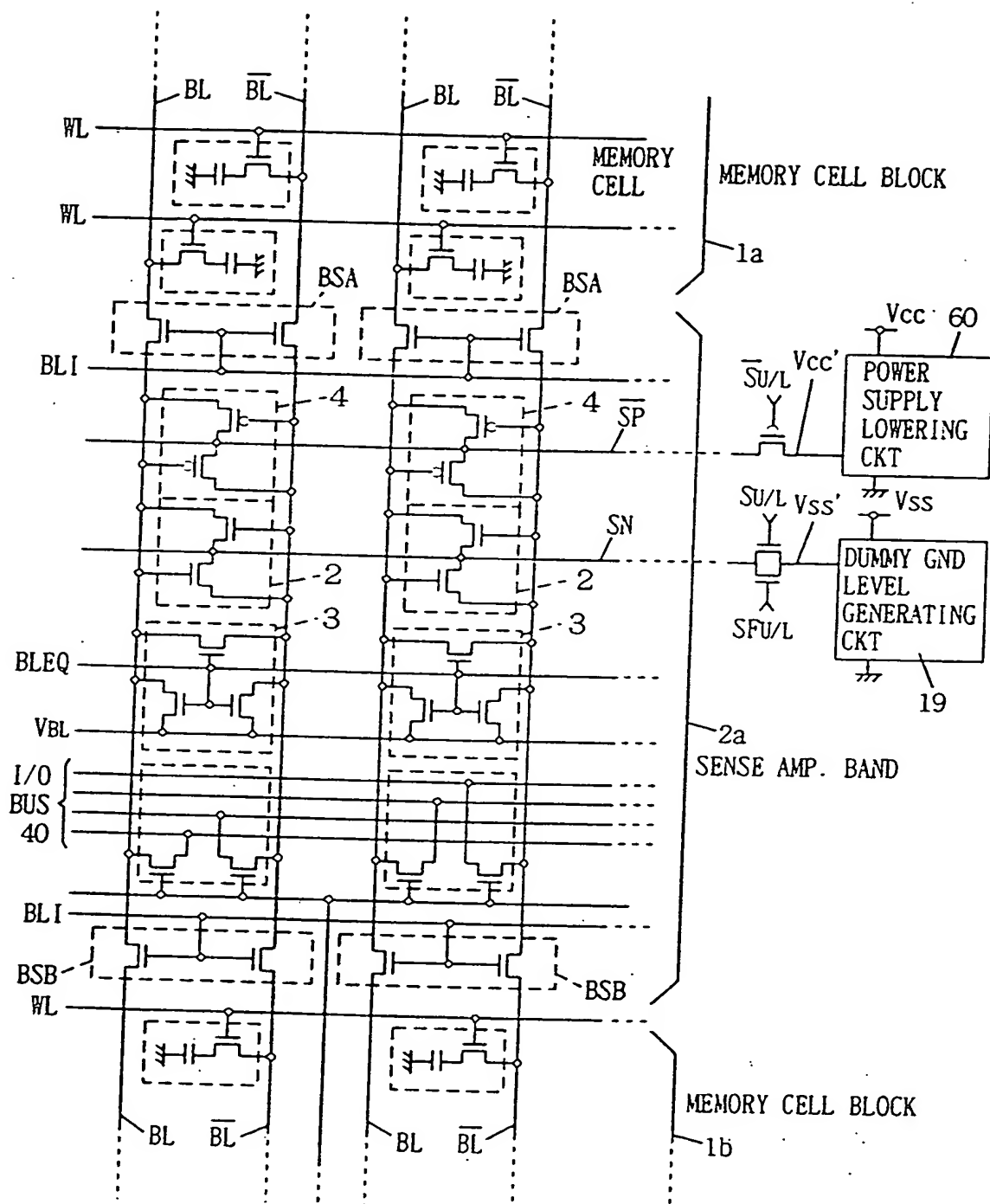
[illegible]

FIG. 43

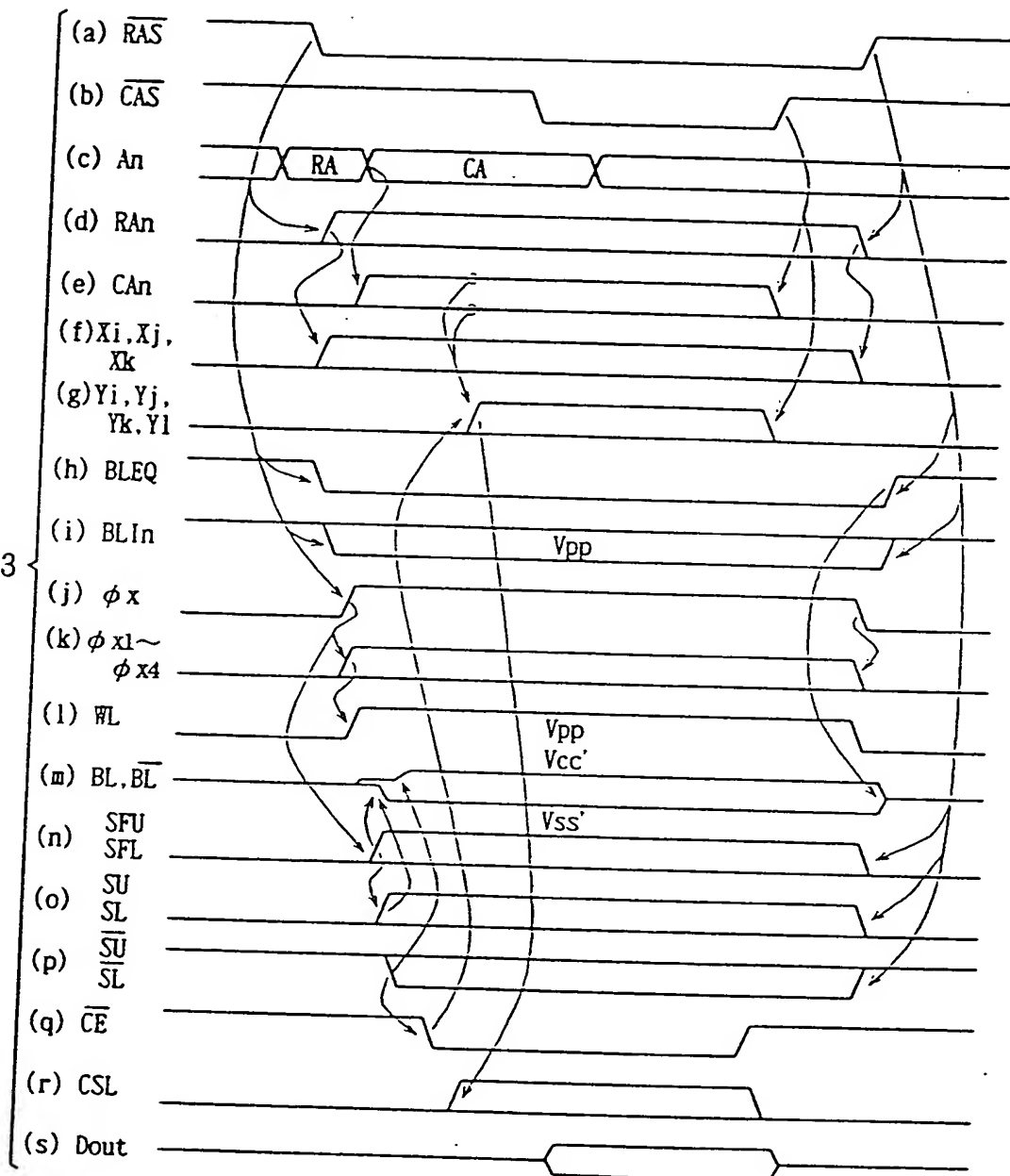


FIG. 44

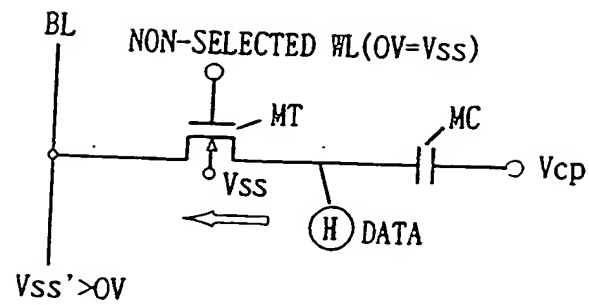


FIG. 45

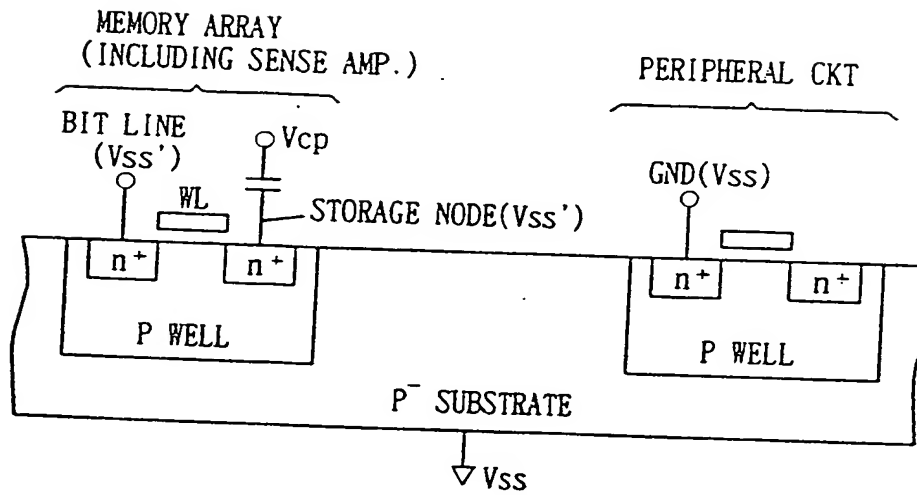


FIG. 46

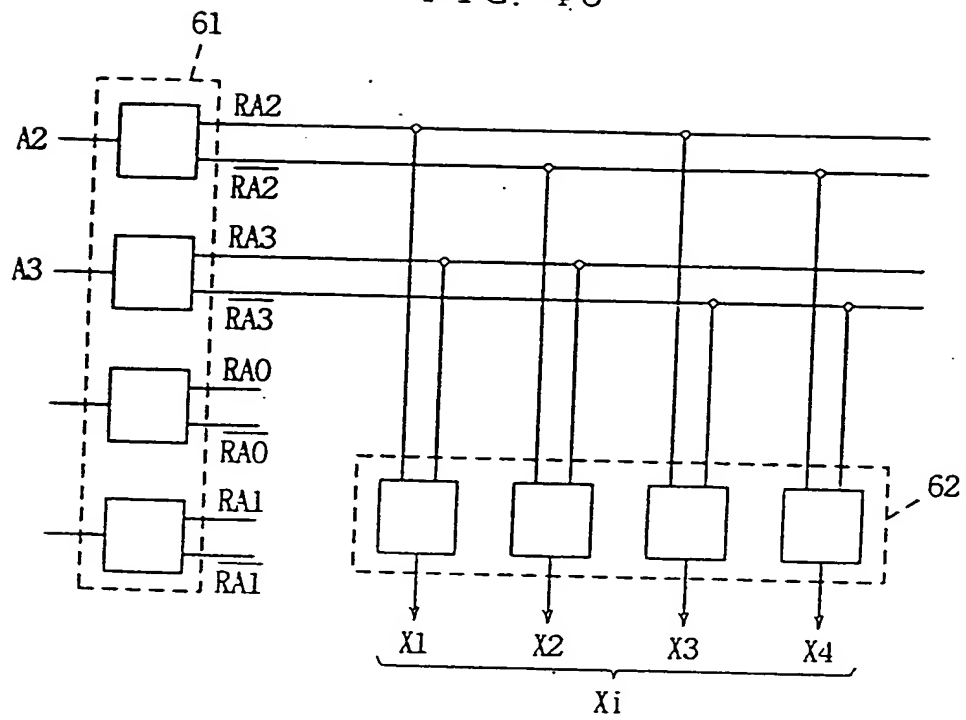


FIG. 47

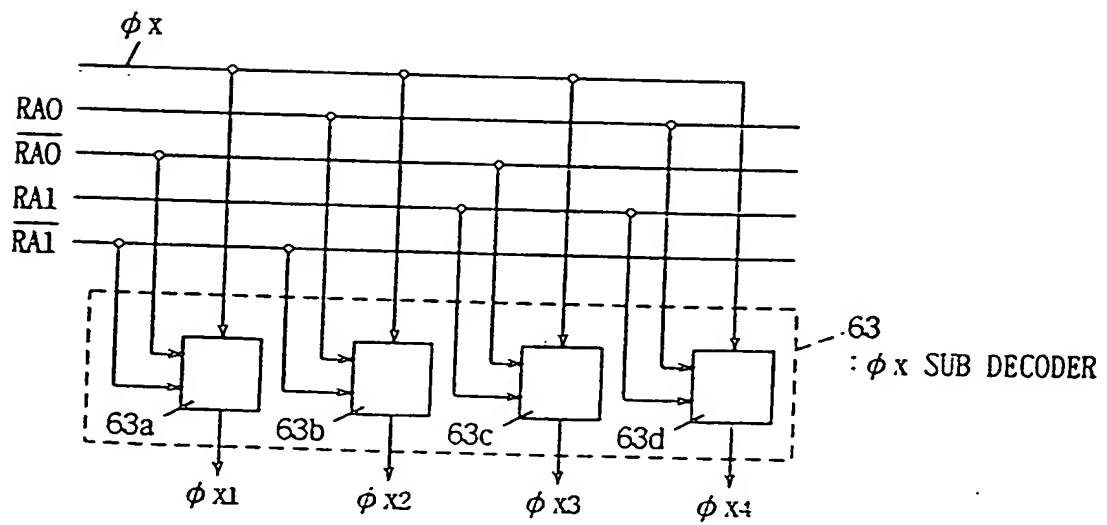


FIG. 48

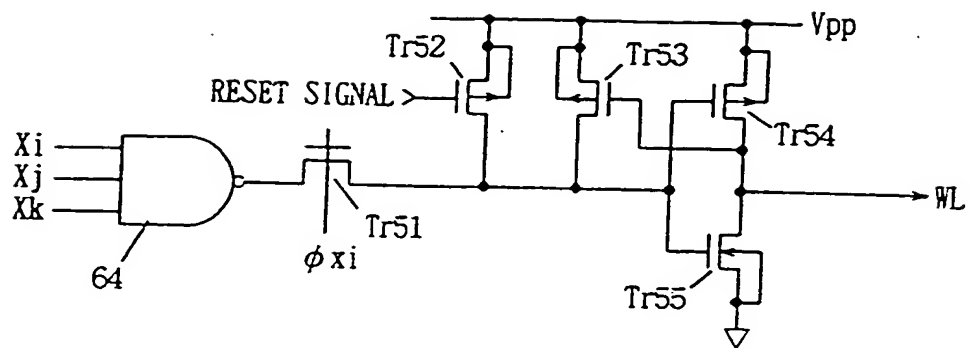


FIG. 49

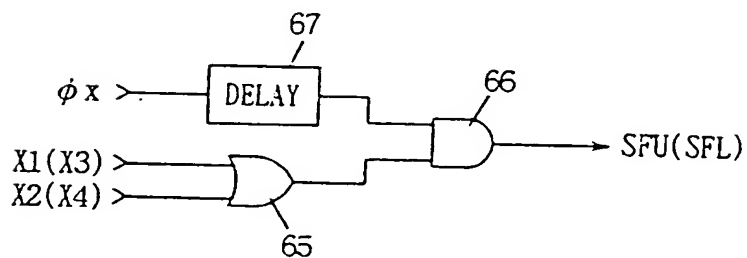


FIG. 50

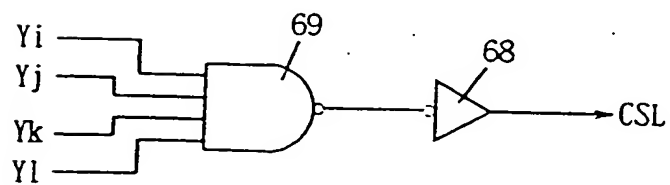


FIG. 51

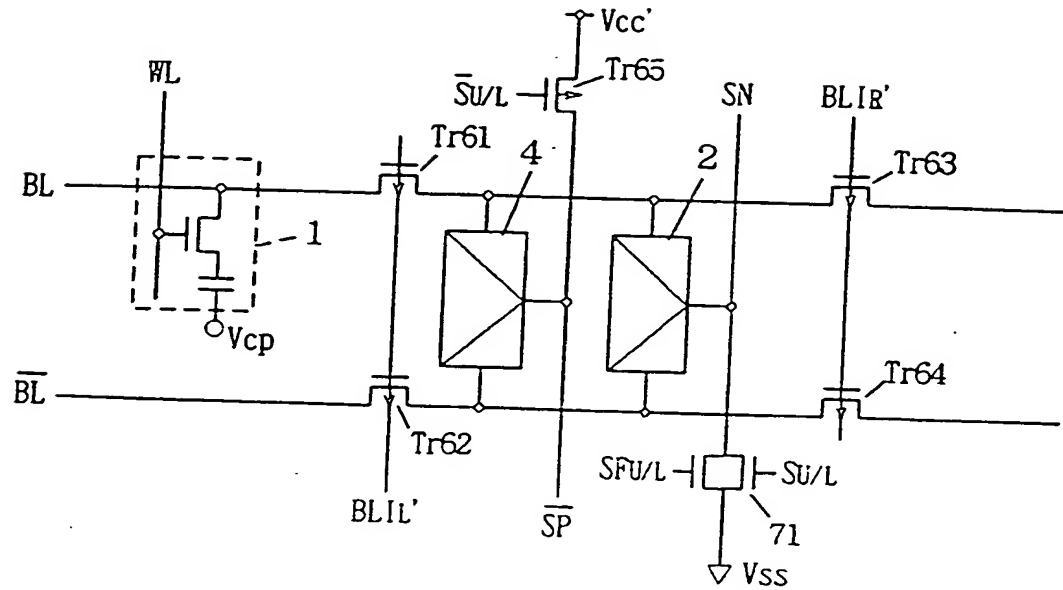


FIG. 52

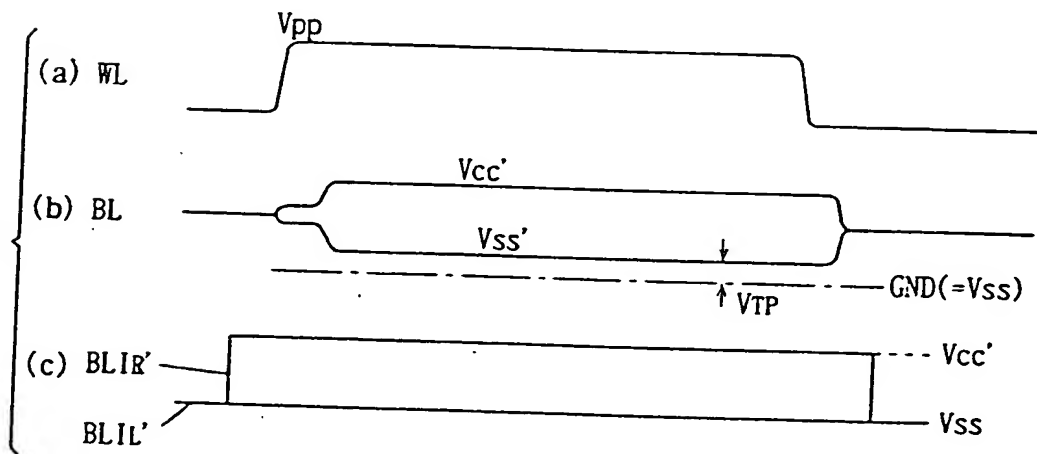


FIG. 54

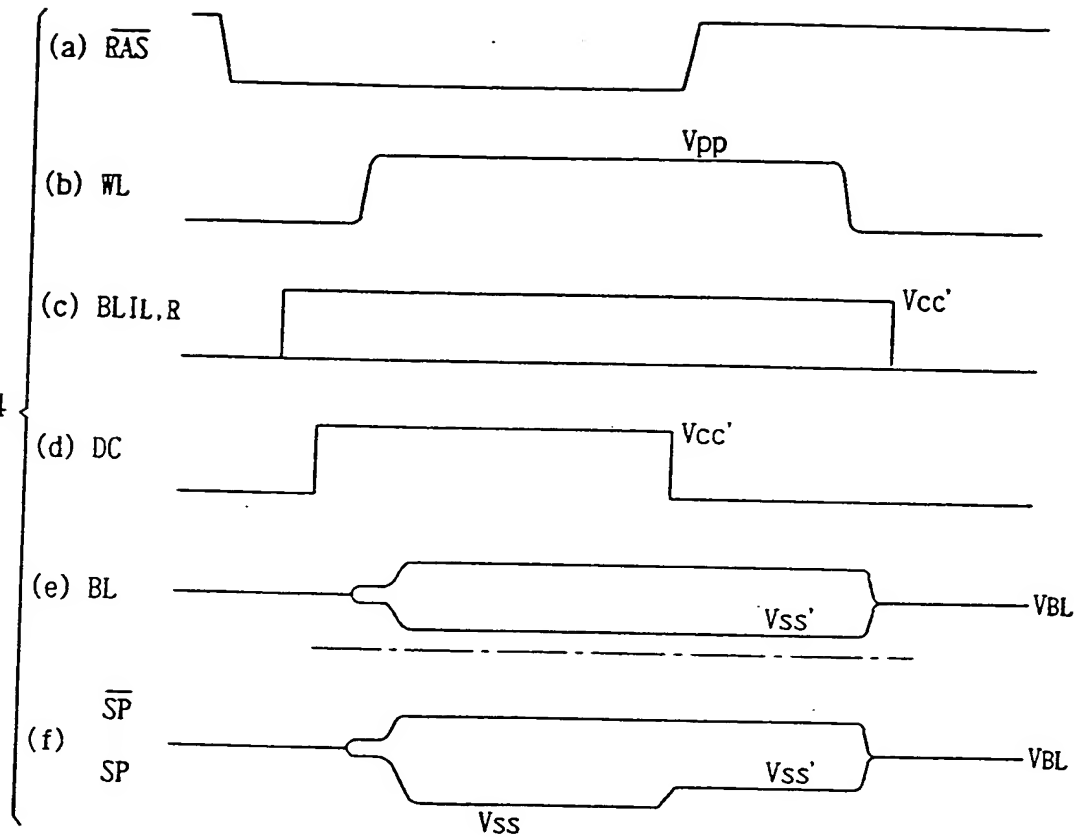
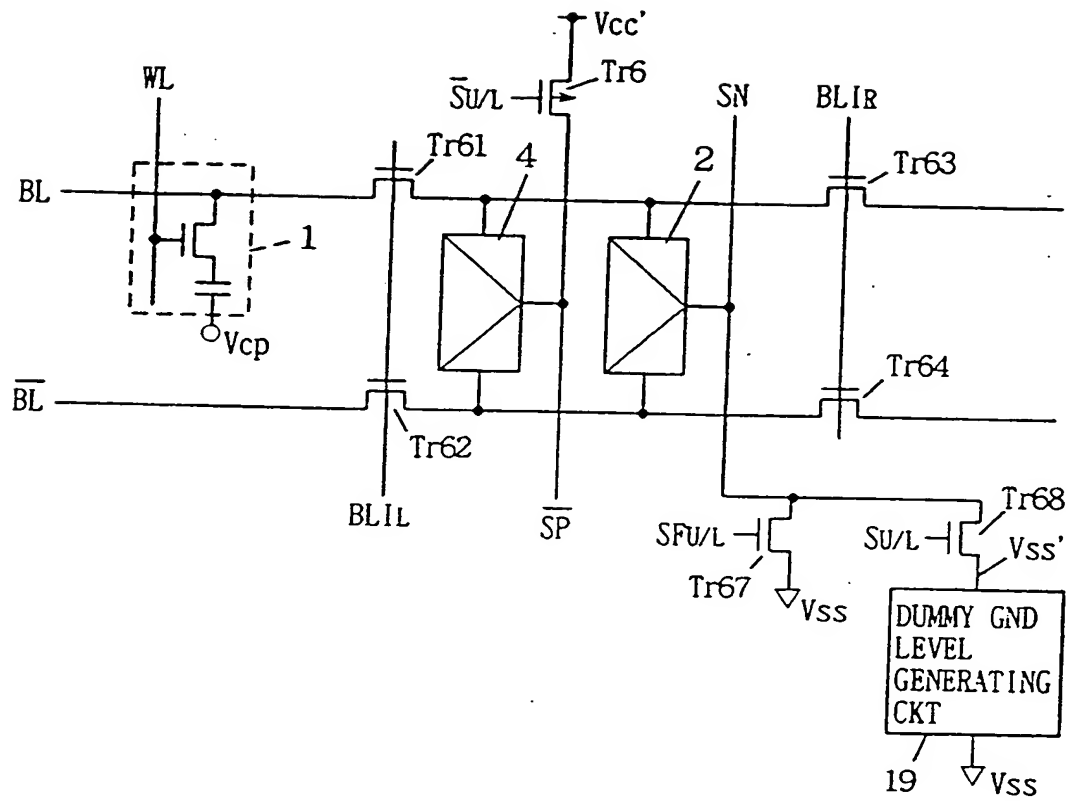


FIG. 55



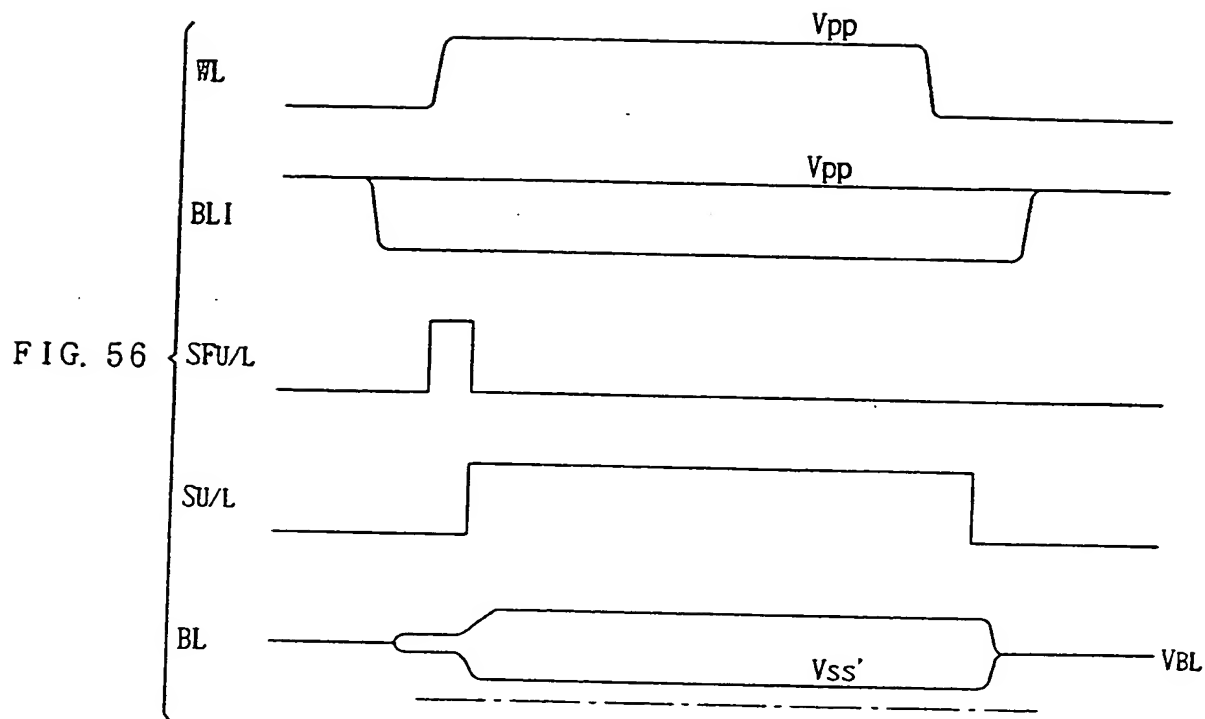


FIG. 57

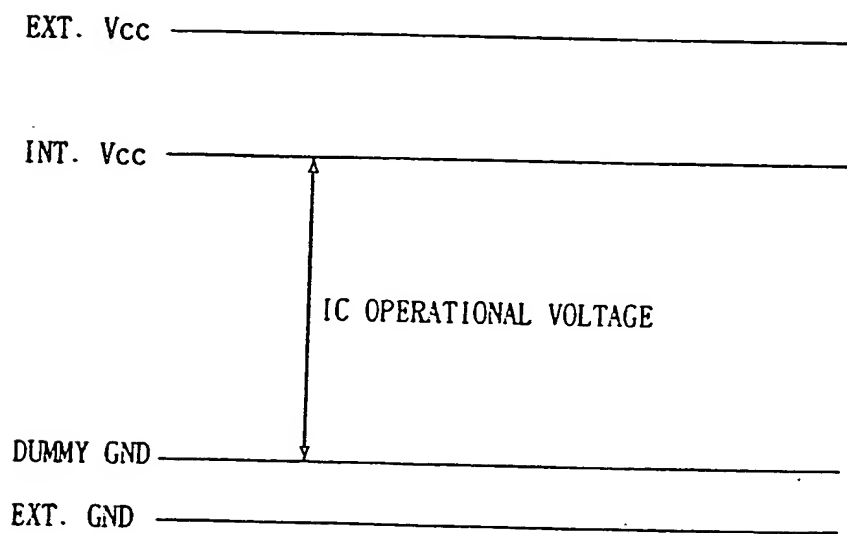


FIG. 58

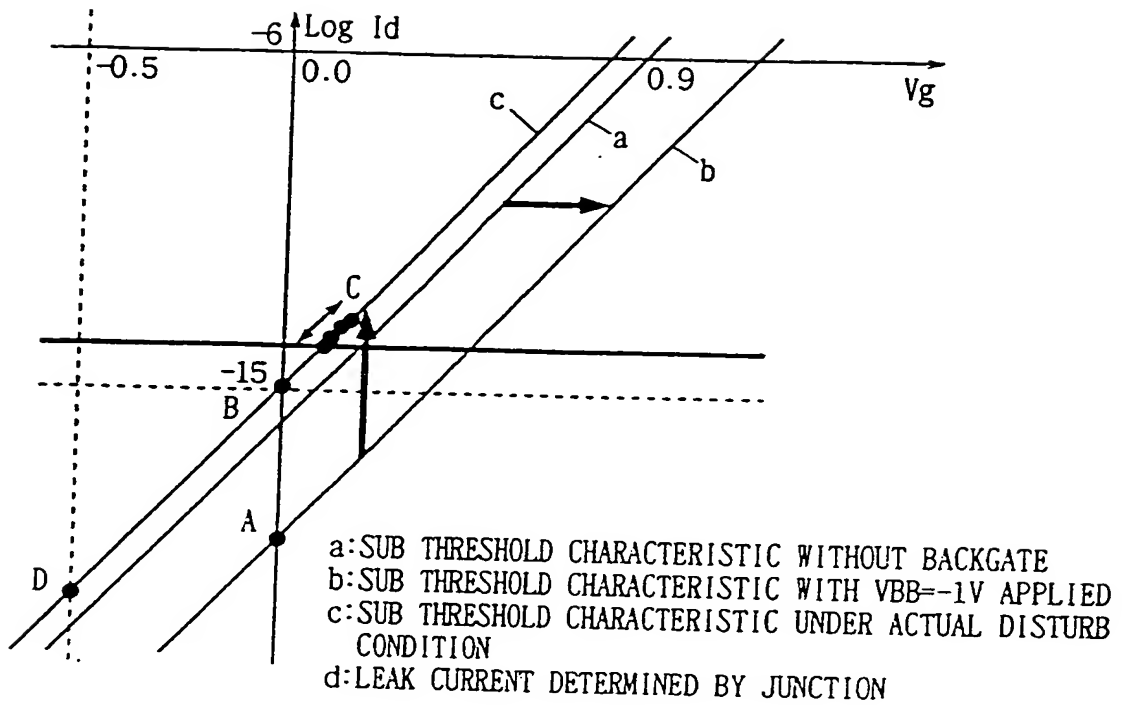


FIG. 59

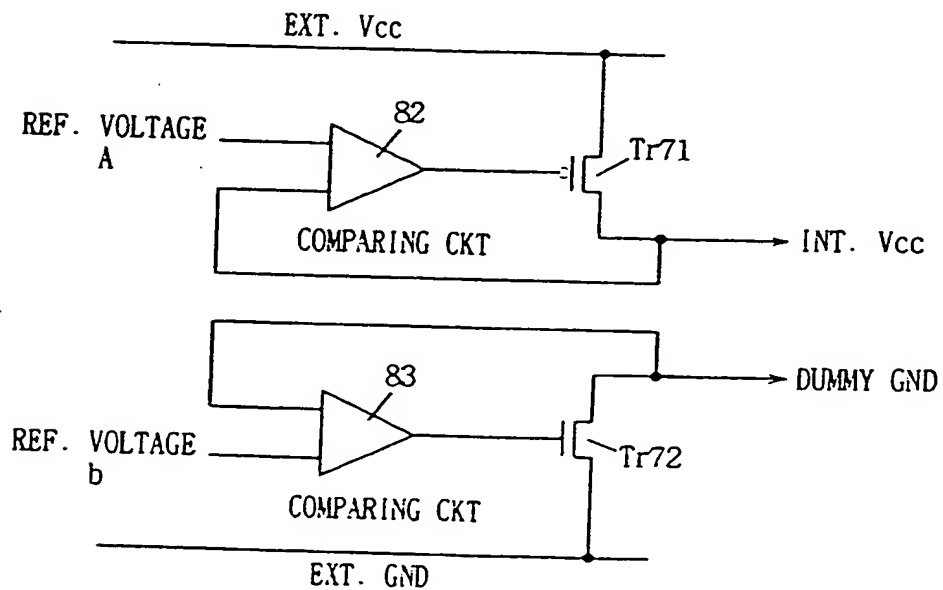


FIG. 60

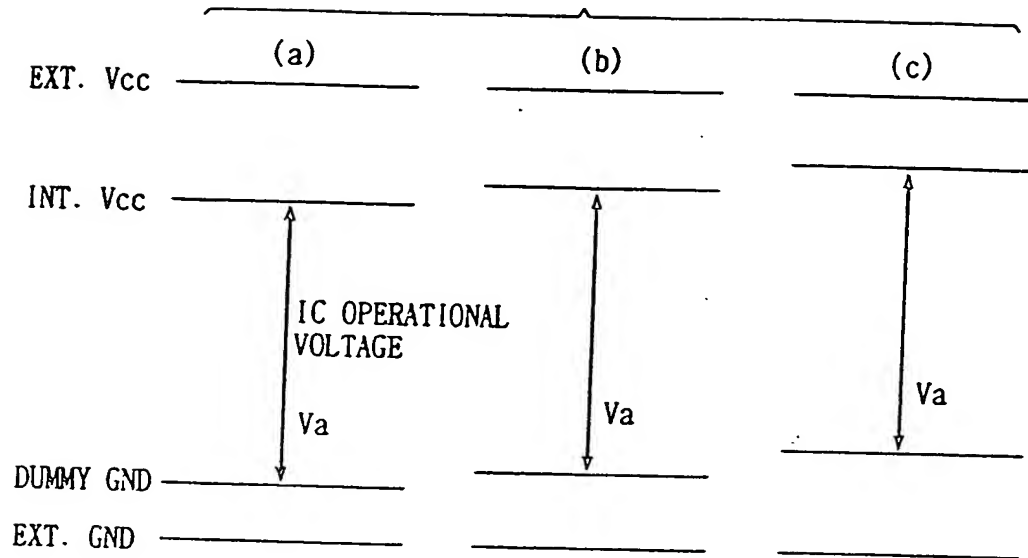


FIG. 61

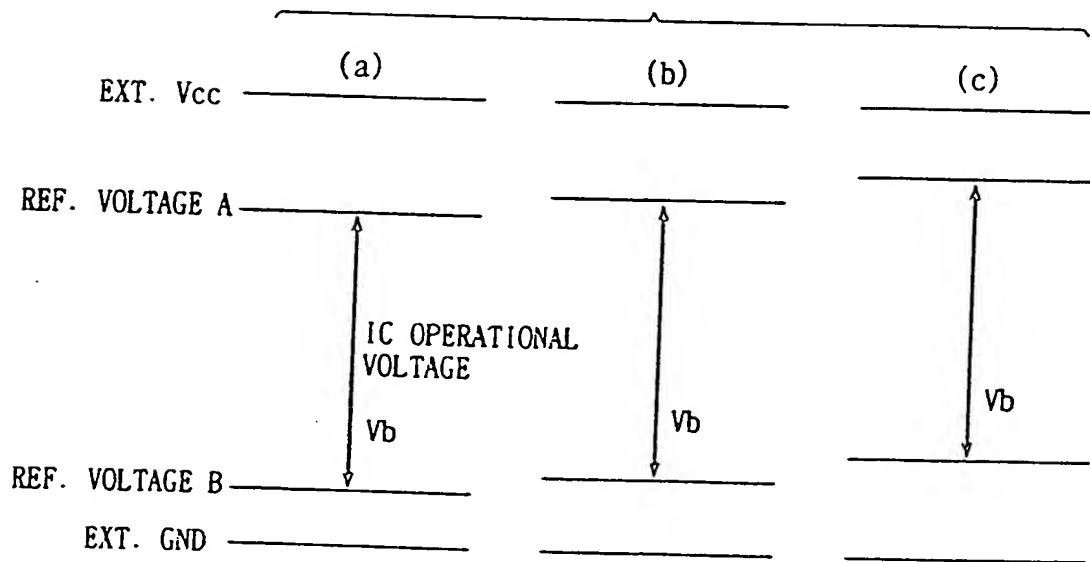


FIG. 62

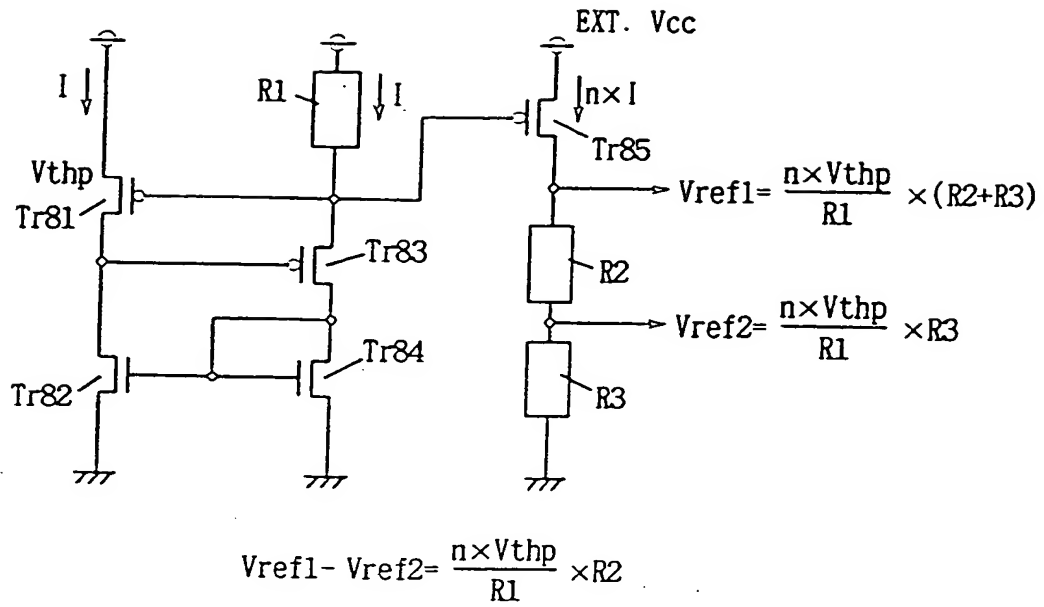


FIG. 63

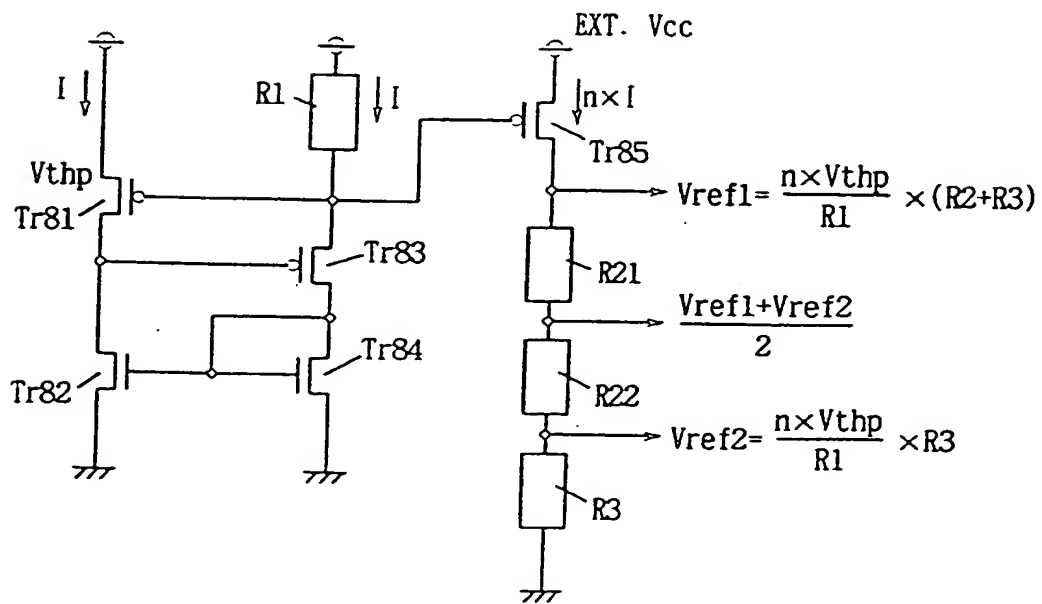


FIG. 64

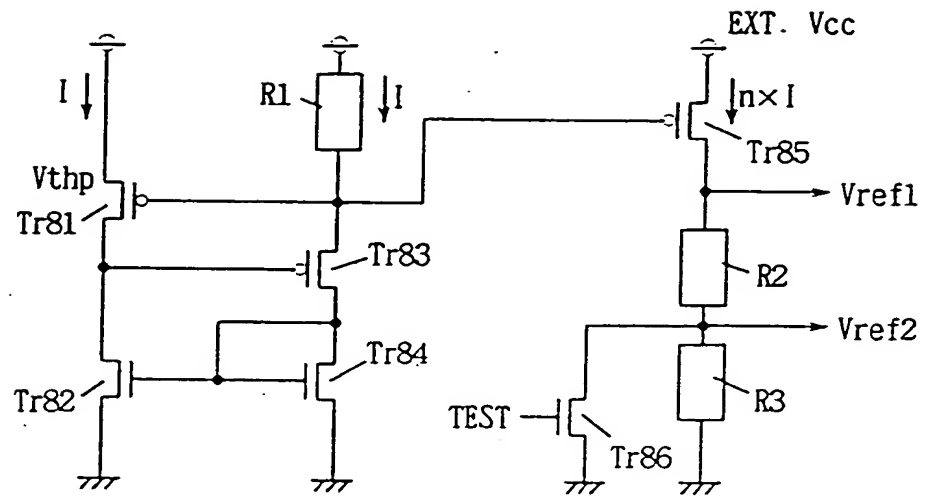


FIG. 65

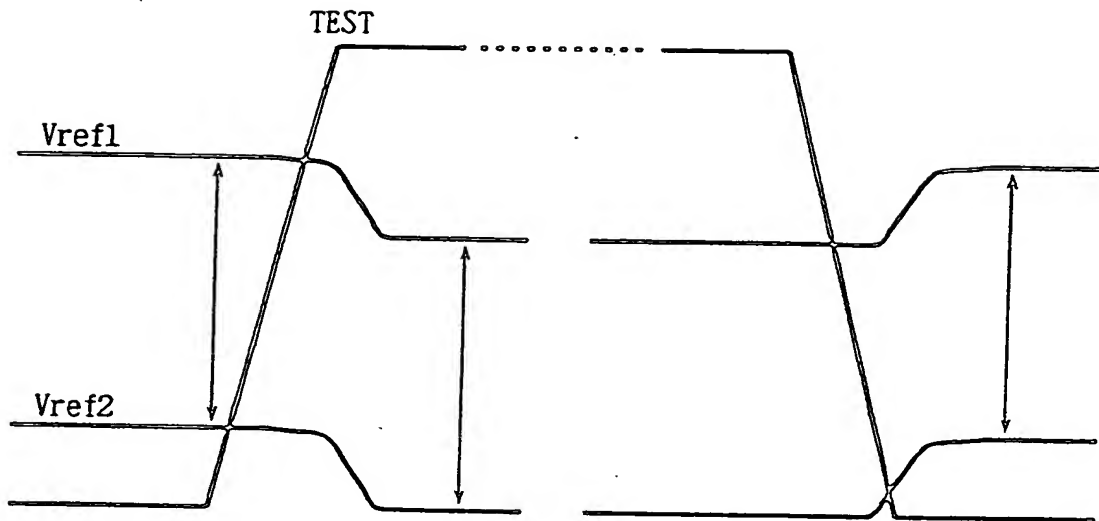


FIG. 66

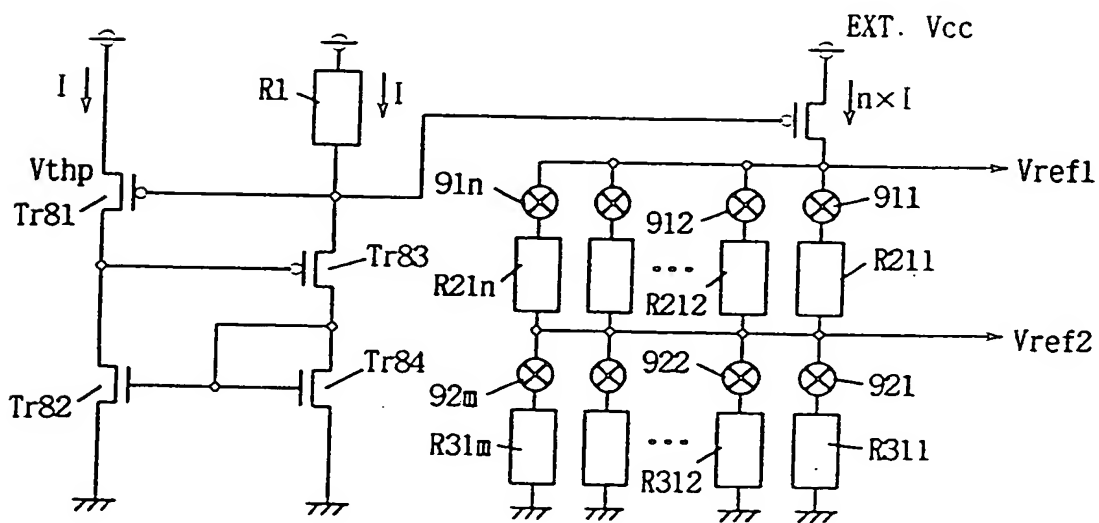


FIG. 67

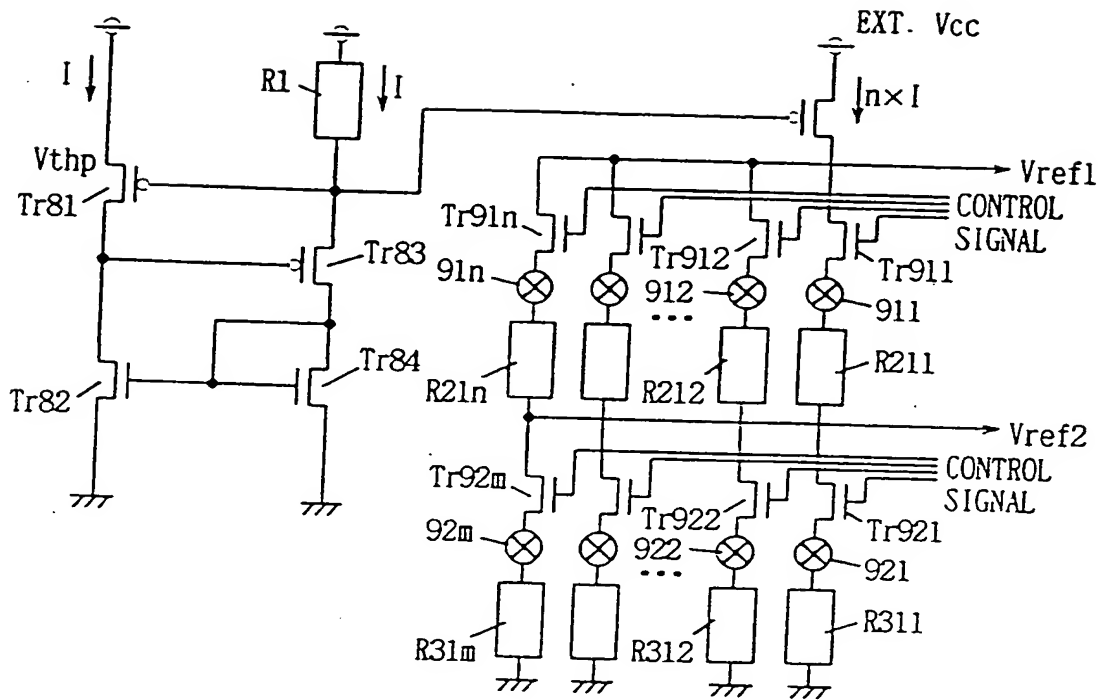
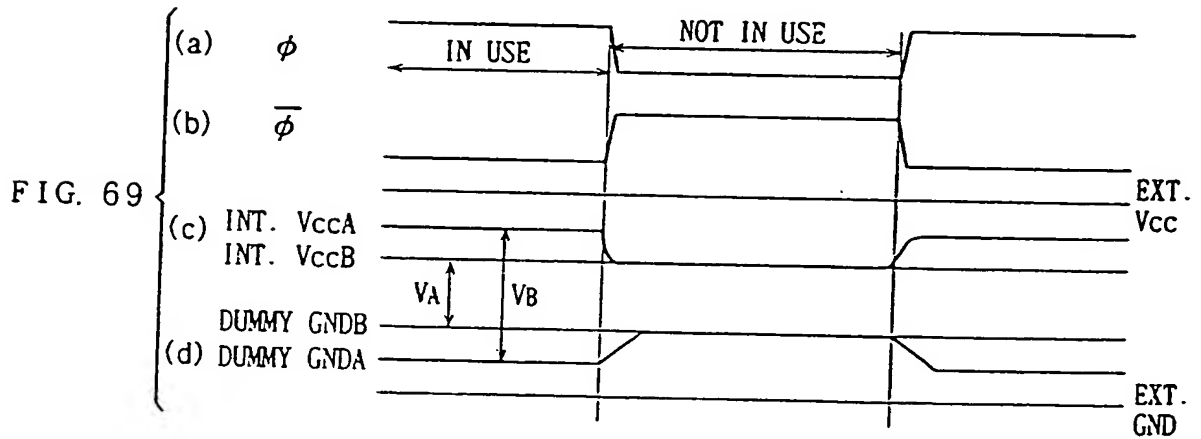
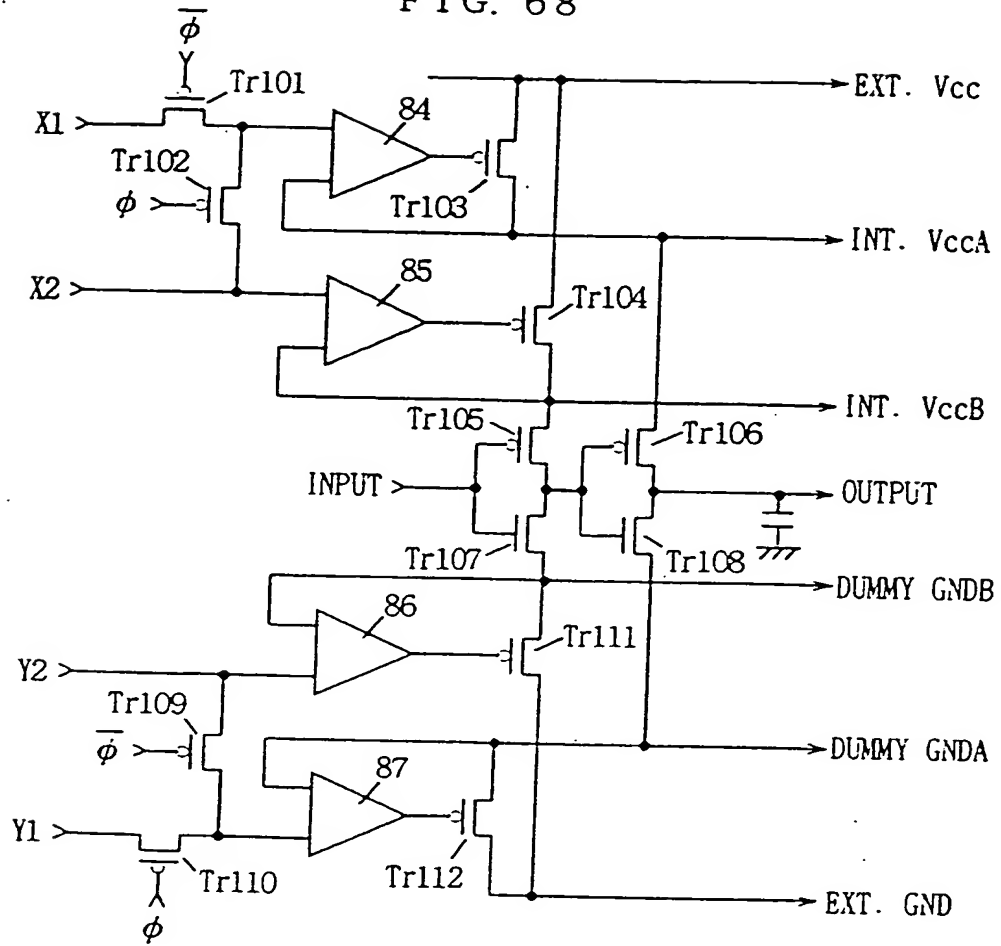


FIG. 68



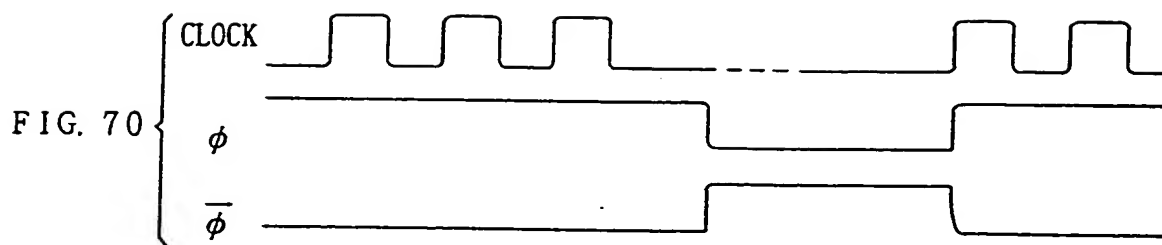


FIG. 71

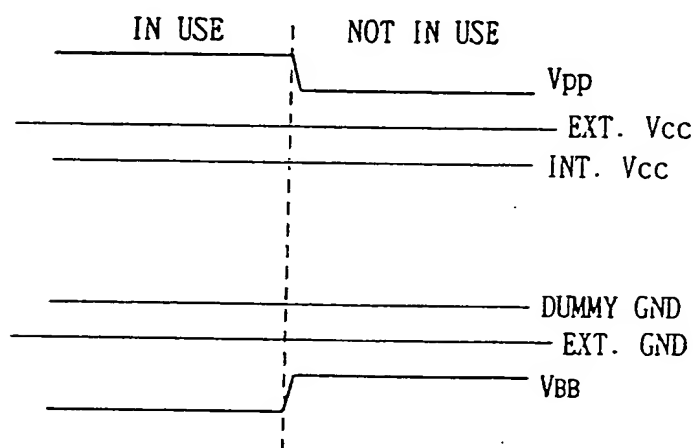


FIG. 72

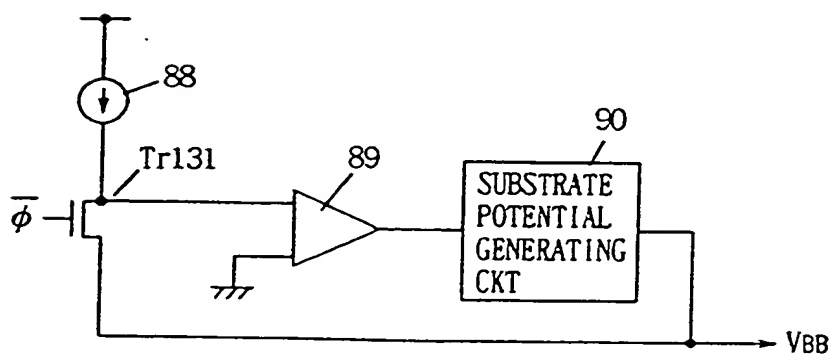


FIG. 73

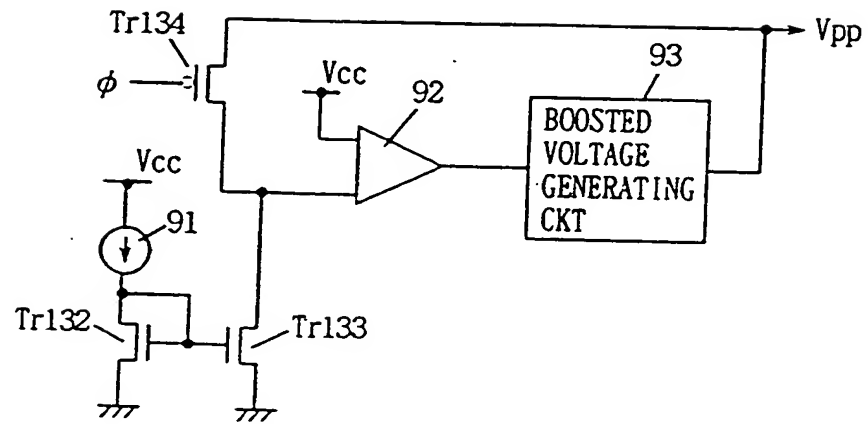


FIG. 74

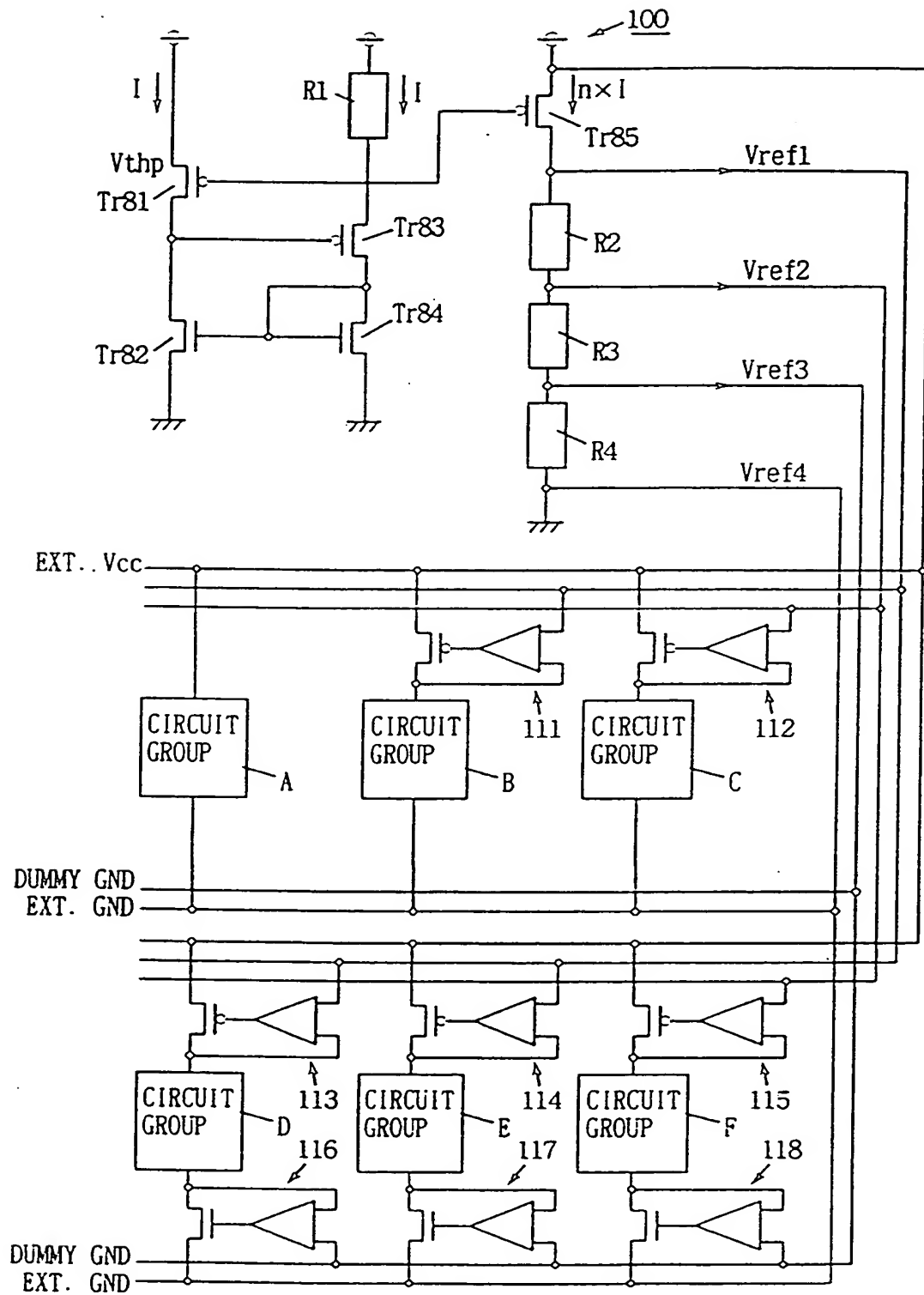


FIG. 75

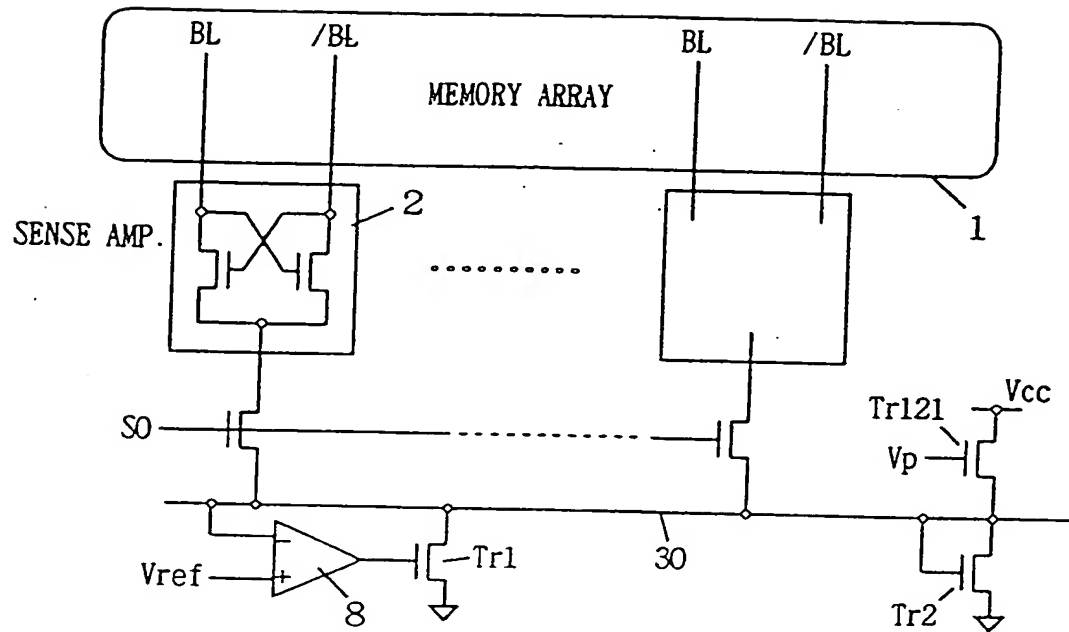


FIG. 76

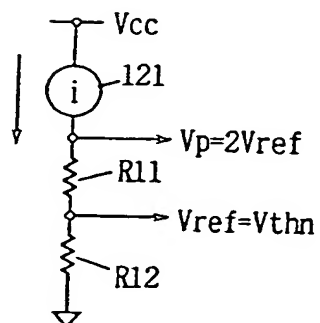


FIG. 77

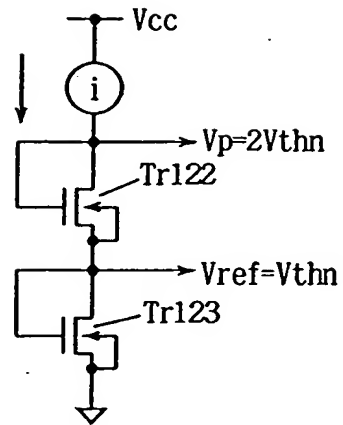


FIG. 78

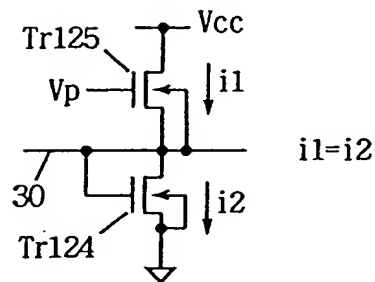


FIG. 79

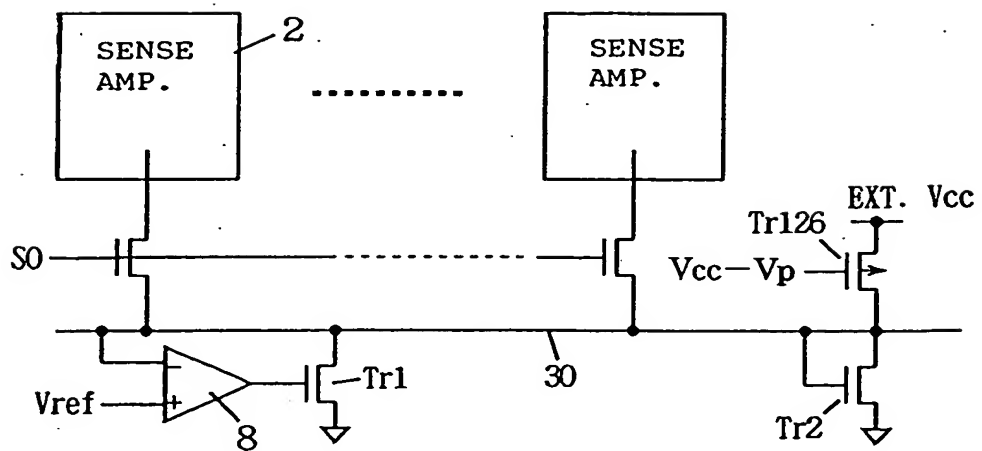


FIG. 80

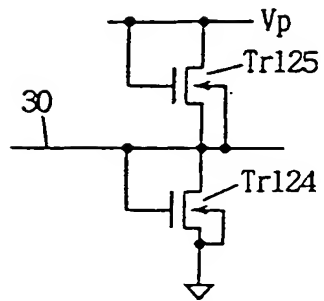


FIG. 81

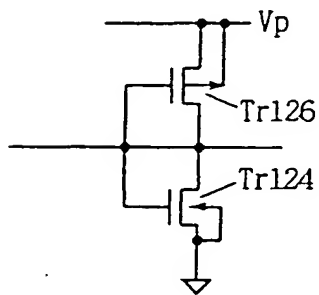
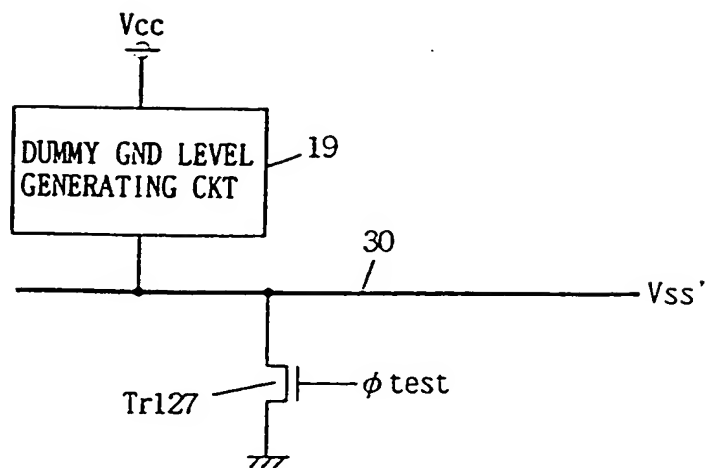


FIG. 82



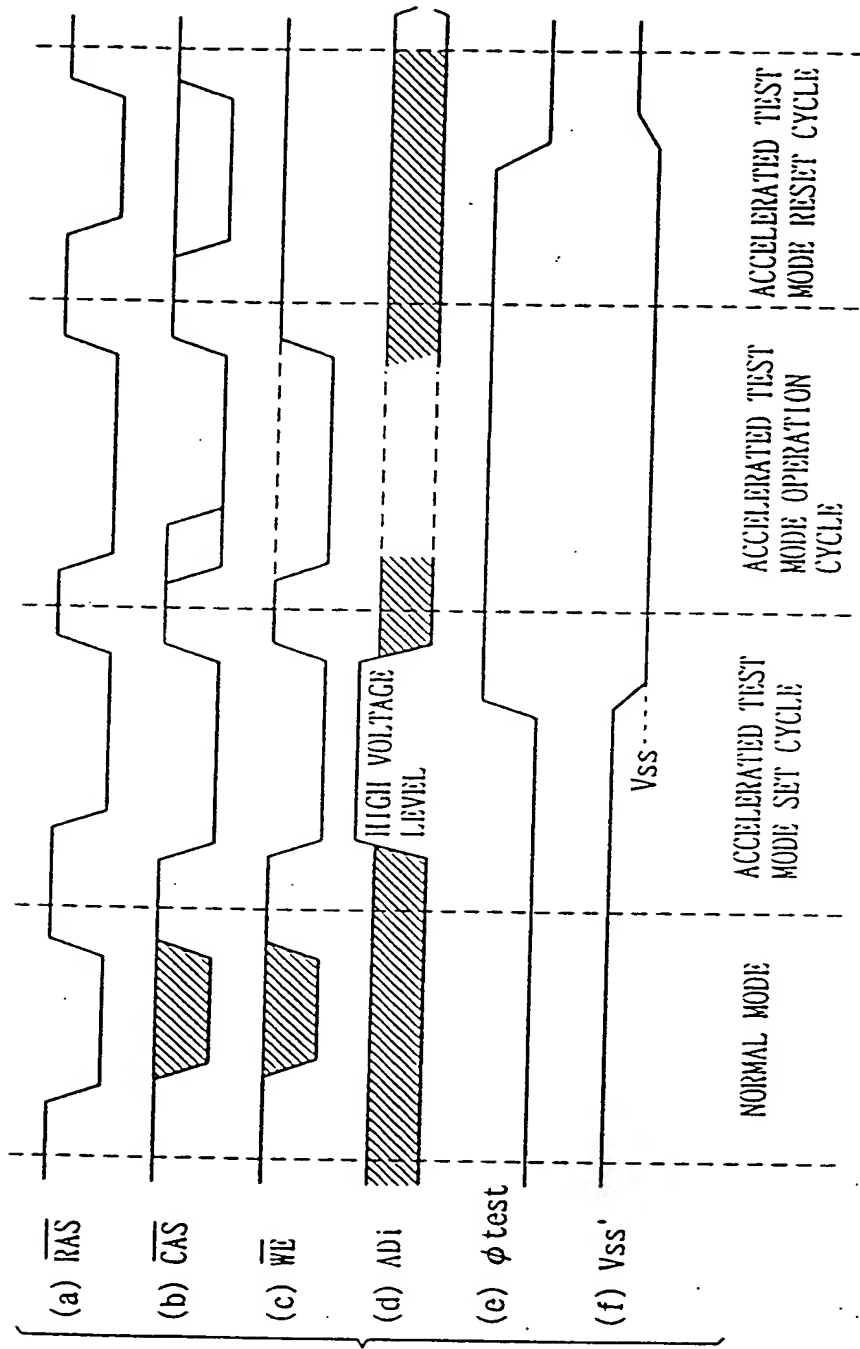


FIG. 83

FIG. 84

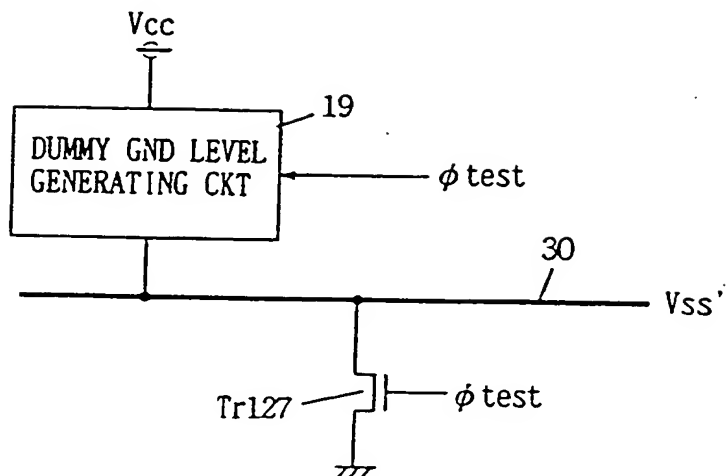


FIG. 85

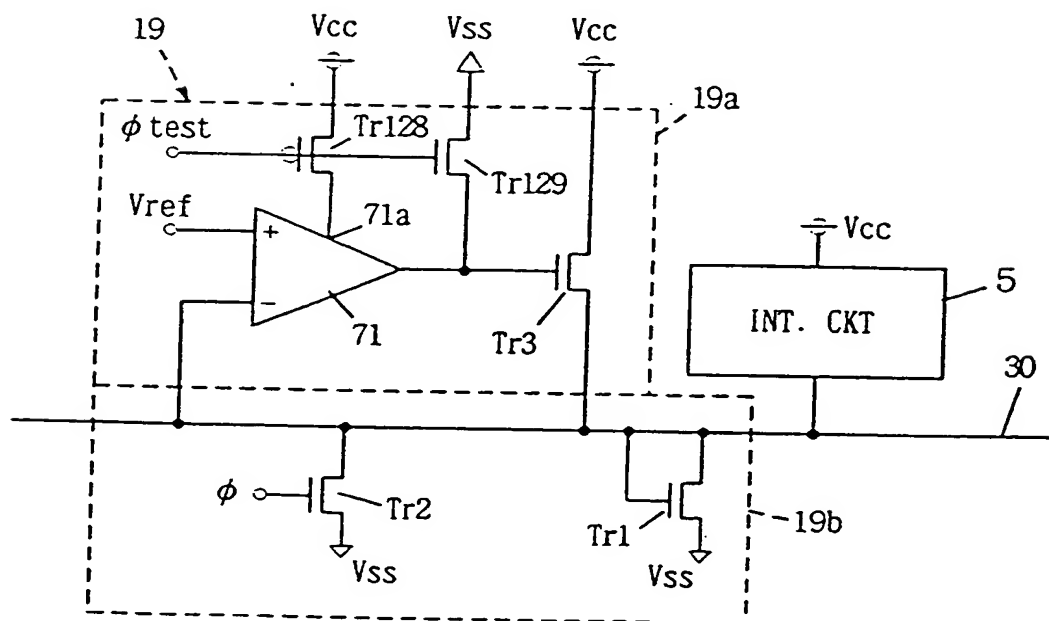


FIG. 86

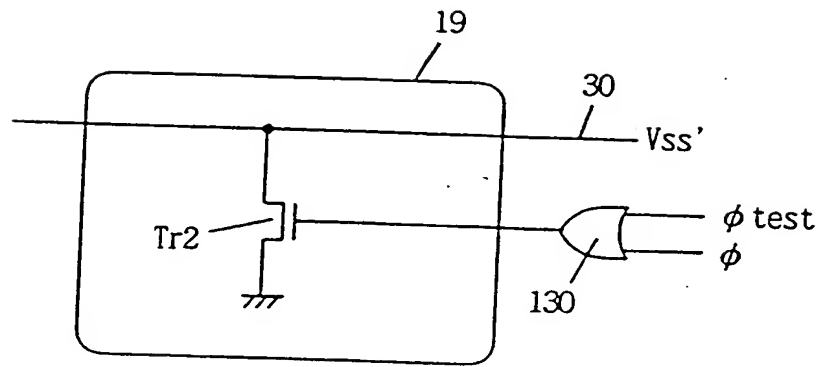
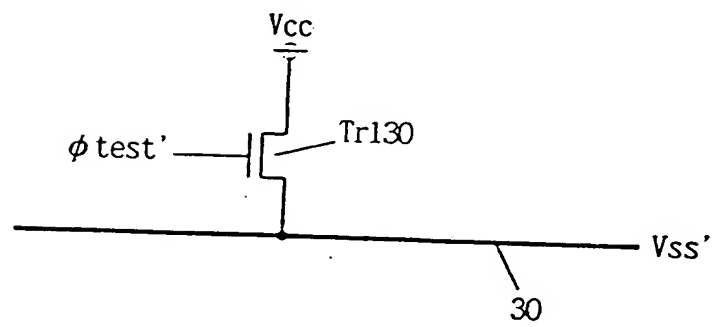


FIG. 87



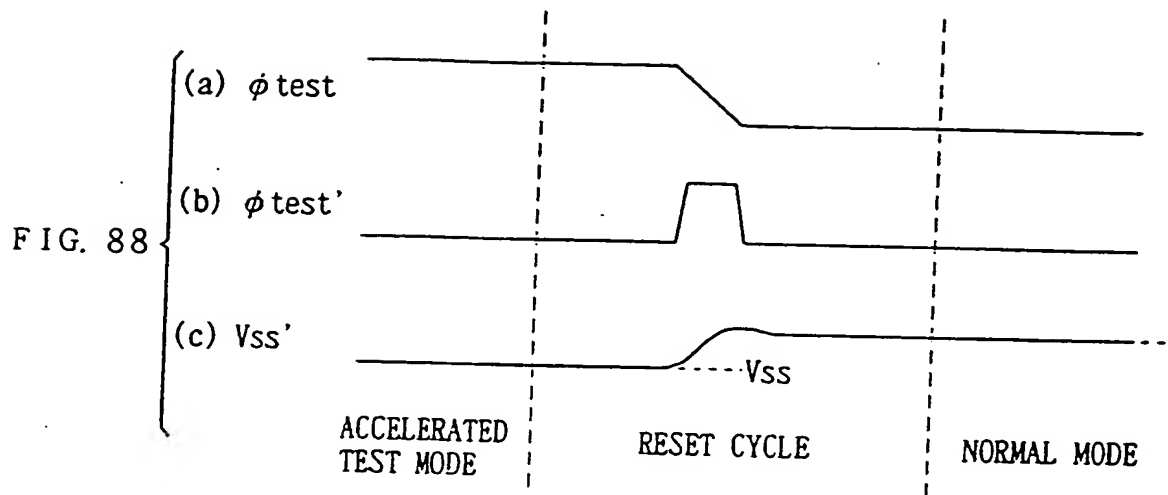


FIG. 89

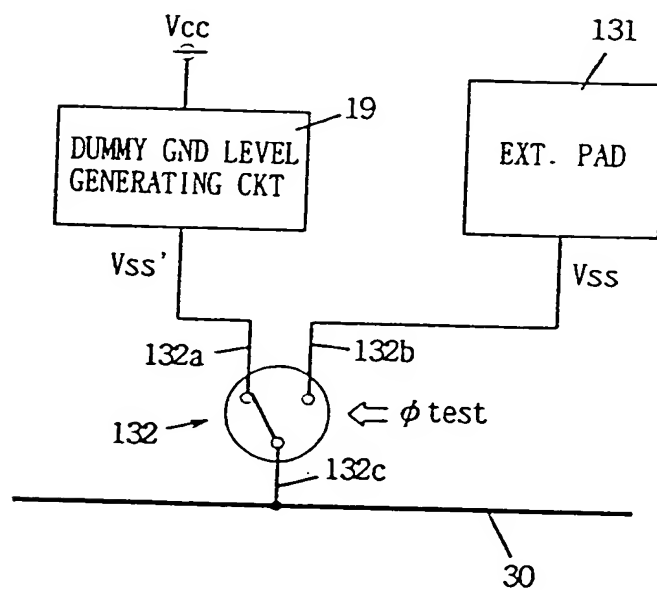


FIG. 90

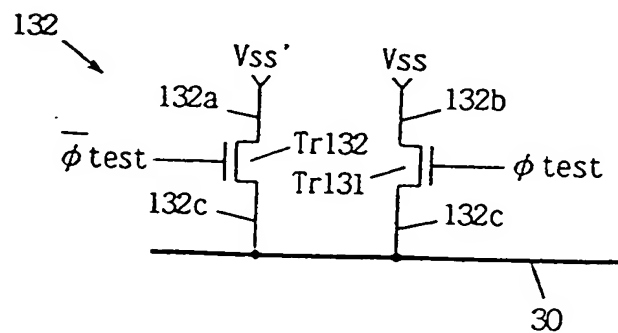
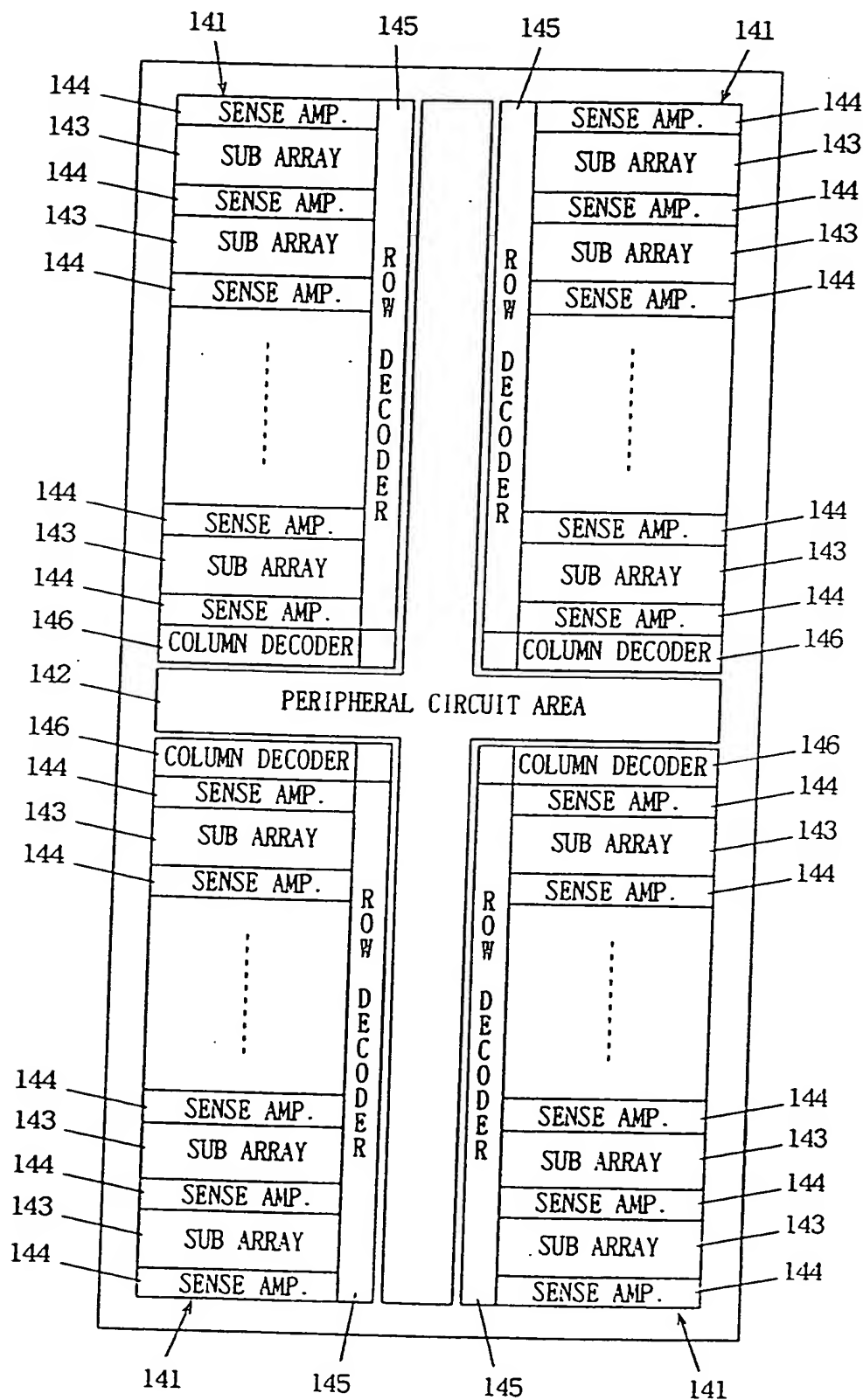


FIG. 91



The diagram illustrates a memory array structure. It features a grid of word lines (BL and BL-bar) and bit lines (SON1 and SON2). Access transistors (Tr131 and Tr132) are connected to the word lines and bit lines. Storage nodes (141, 143, 144) are connected to the word lines. The array is divided into sections by dashed lines, indicating a repeating pattern. The bit lines are connected to a common source line (SON1) and a common drain line (SON2). The word lines are connected to a common gate line (Vss) and a common gate line (Vss'). The storage nodes are connected to the word lines and the common gate line (Vss').

```

graph LR
    SON[SON] --- NAND161[161]
    test[ø test] --- NAND161
    NAND161 --- SON1[SON1]
  
```

FIG. 95

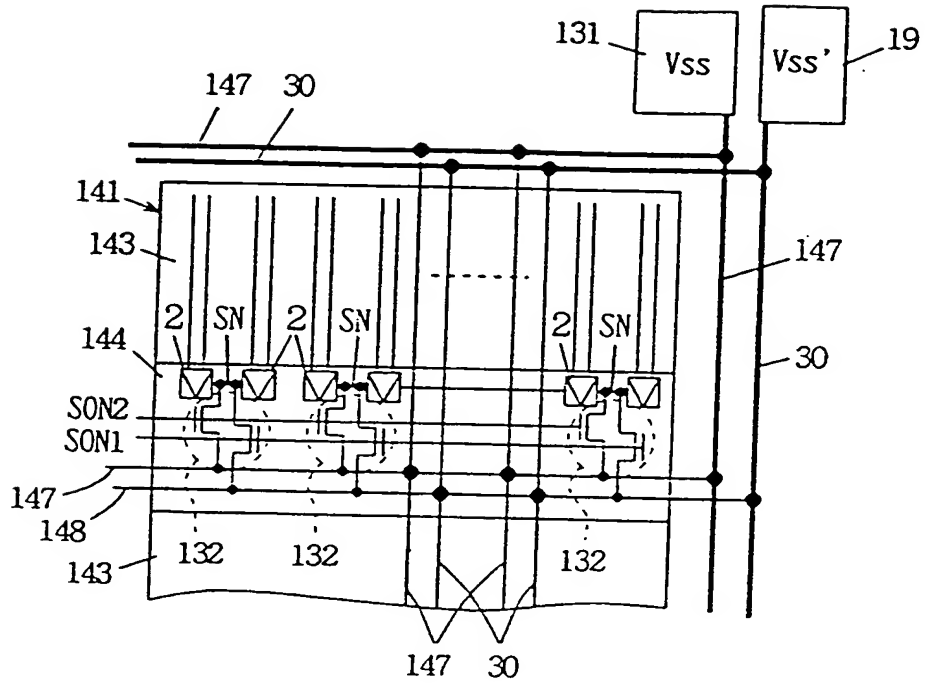


FIG. 96

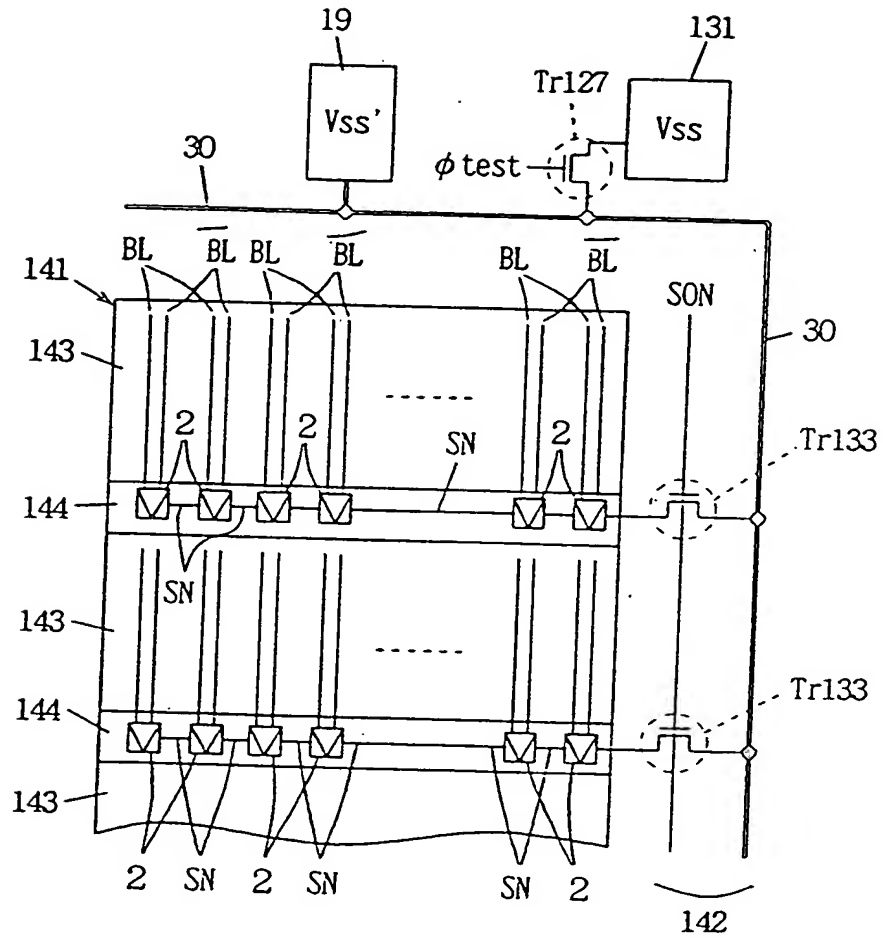


FIG. 97

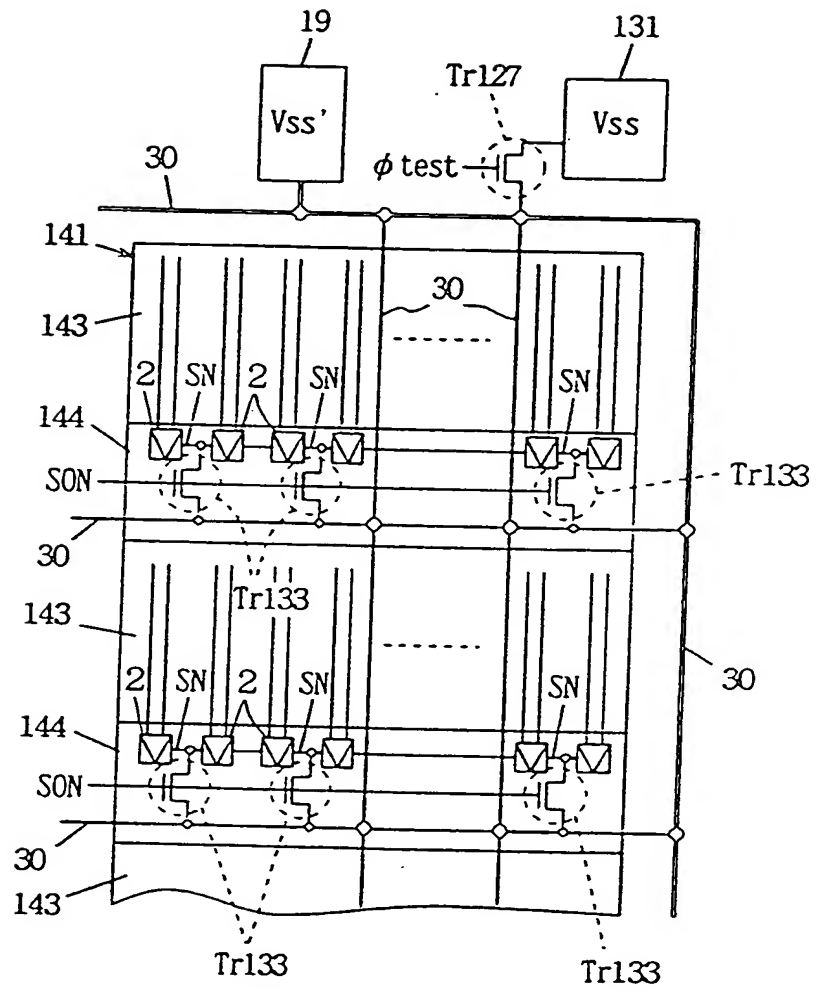


FIG. 98

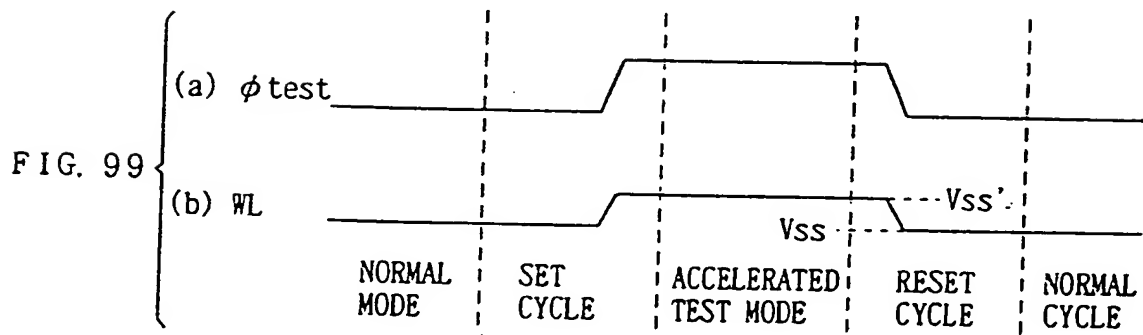
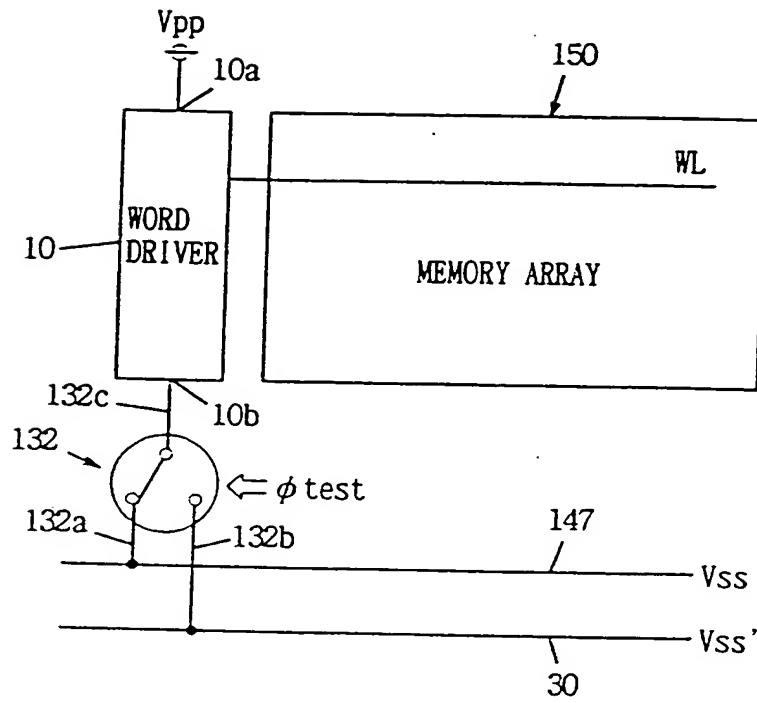


FIG. 100

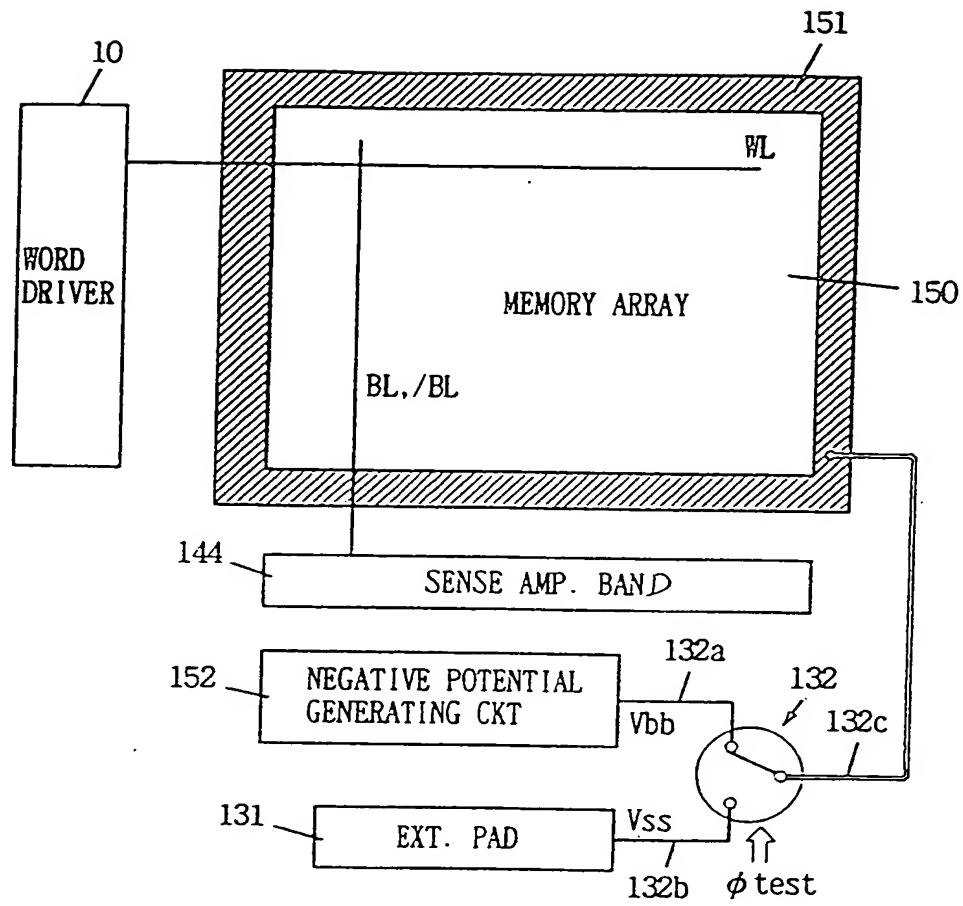


FIG. 101 PRIOR ART

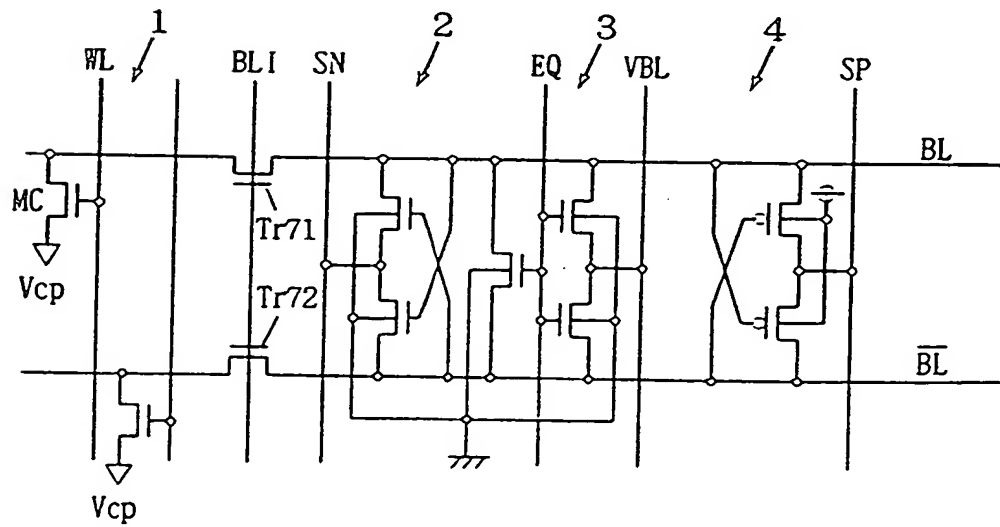


FIG. 102
PRIOR ART

